

## Verification of Real-Time Systems SS 2015

### Assignment 10

*Deadline: July 9, 2015, before the lecture*

#### Exercise 10.1: Microarchitectural Analysis (3+3+1=7 Points)

- (a) Familiarise yourself with different types of pipeline designs such as in-order, VLIW (Very Long Instruction Word), and out-of-order design. Briefly discuss advantages and disadvantages of the respective designs. Name at least 3 items per design.
- (b) Explain how abstraction introduces non-determinism into the microarchitectural analysis. Provide at least three examples.
- (c) What should the initial analysis information for microarchitectural analysis be?

#### Exercise 10.2: Path Analysis (3+3=6 Points)

- (a) How can we encode information about infeasible paths into the (traditional and state-sensitive) path analysis? Consider the example on slide 6, Path Analysis. Perform your proposed encoding for this example. *Note:* This fragment could be executed in a loop.
- (b) Formulate the generic loop constraint for state-sensitive path analysis.

#### Exercise 10.3: Persistence Analysis for Non-LRU Policies (3+3+8=14 Points)

- (a) Give an example that the block-wise miss competitiveness result for MRU is tight for MRU(4) and LRU(4), i.e. a persistent block in LRU(4) can cause up to 4 misses in MRU(4).
- (b) Formulate the constraints that are necessary to incorporate the above “persistence information” for MRU into the path analysis. Which information needs to be exposed in the microarchitectural execution graph (an example of such a graph is given on slide 12, Path Analysis)?
- (c) *Hard:* Can we incorporate similar “persistence information” for FIFO caches? Which information needs to be exposed in the microarchitectural execution graph? Formulate the constraints that are necessary.