Write-Back Caches in WCET Analysis

ECRTS 2017

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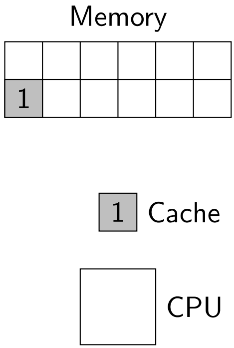
COMPUTER SCIENCE

Roadmap

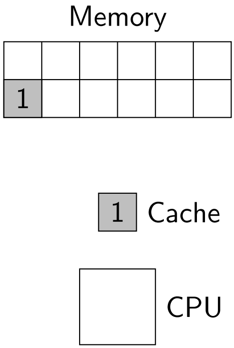
- Background
- Write-back Analysis
  - Eviction-focussed Analysis
  - Store-focussed Analysis
- Evaluation
- Conclusion and Future Work

Write-back Caches



Memory Accesses: 0

Write through



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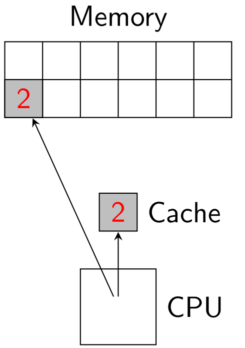

Memory Accesses: 1

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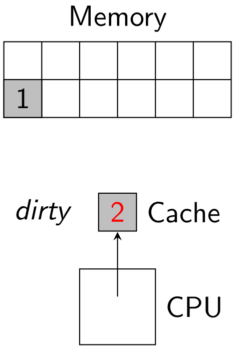

Memory Accesses: 0

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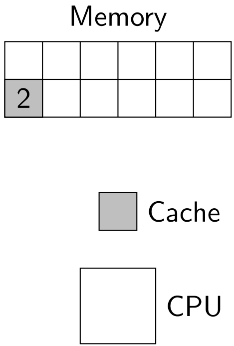

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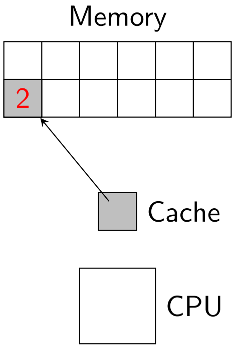

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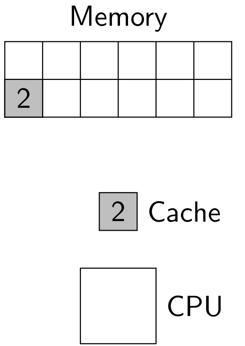

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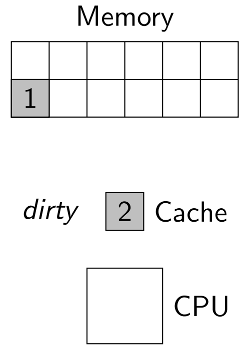

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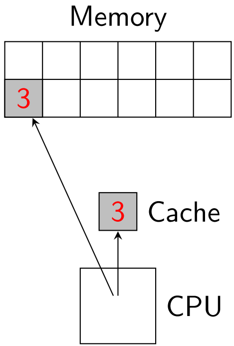
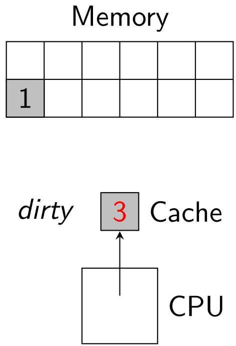
Write back

Write-back Caches



Memory Accesses: 2

Write through



Memory Accesses: 0

Write back

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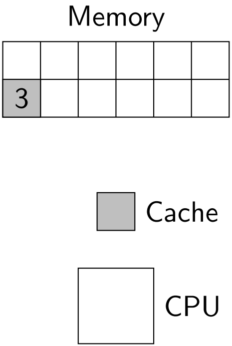

Memory Accesses: 2

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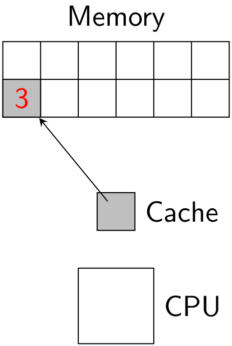

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Write back

Motivation and Challenge

The Good: write back delivers higher performance

The Ugly: write back requires more sophisticated analysis

> *"for real systems, write-through seems to always result in lower worst-case estimates"* Wilhelm et al. (2010)

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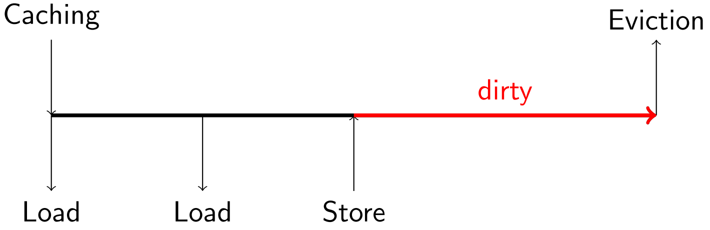
Major Events in the Life of a Cache Block

Eviction-Focused Analysis
Eviction causes write back



Store-Focused Analysis
store causes write back later

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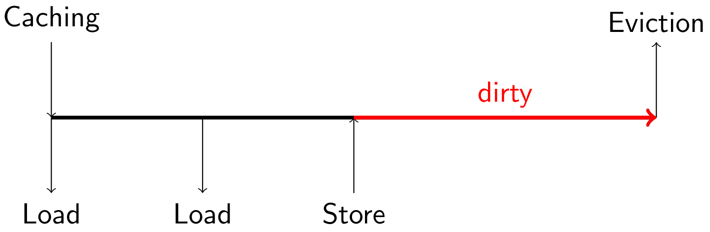

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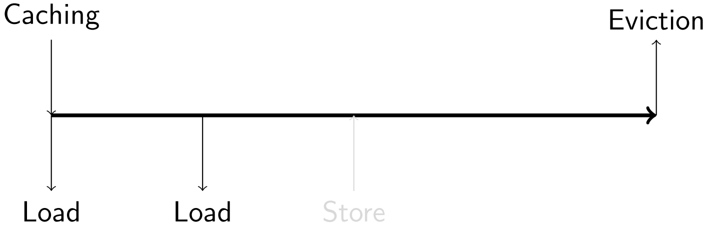

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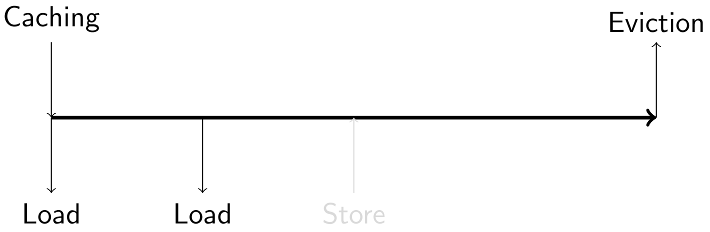
Eviction-Focused Analysis
Eviction causes write back if there was a store



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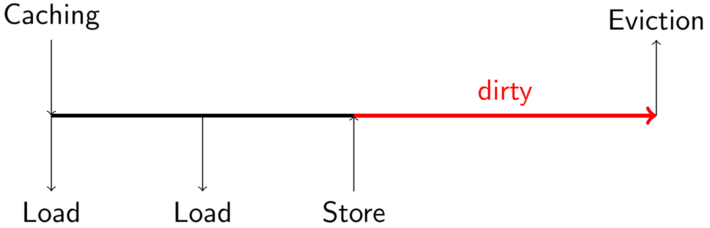

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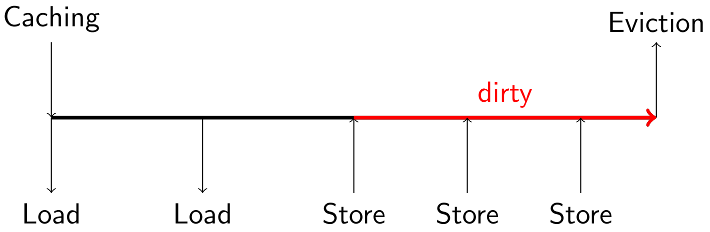

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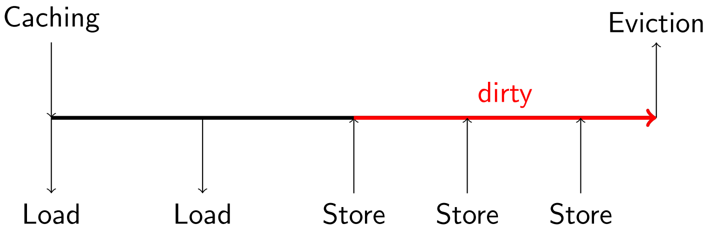
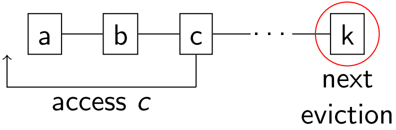


Store-Focused Analysis
Dirtifying store causes write back later

Least-Recently-Used Replacement (LRU)



Example

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x = f(x)
sum = 0
repeat up to N times
    sum += arr[read_sensor()]
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                ↑
    may evict x in any iteration
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Example

dirtifying stores → x = f(x), sum = 0

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sum = 0
repeat up to N times
    sum += arr[read_sensor()]
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↑ (read_sensor()) may evict *x* in *any* iteration

Persistence Analysis

int arr[M]
repeat up to N times
    arr[read_sensor()]++

Assume the array is smaller than the cache

$\Longrightarrow$ at most M dirtifying stores, independently of N

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Evaluation

1. Write back vs write through
2. Precision of write-back analysis
3. Store-focussed analysis vs eviction-focussed analysis

Evaluation setup

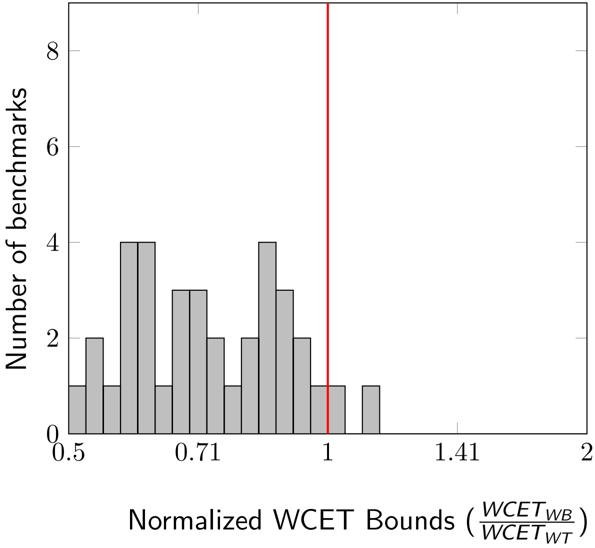
Benchmarks

- Mälardalen benchmark suite
- 5 *SCADE* benchmarks

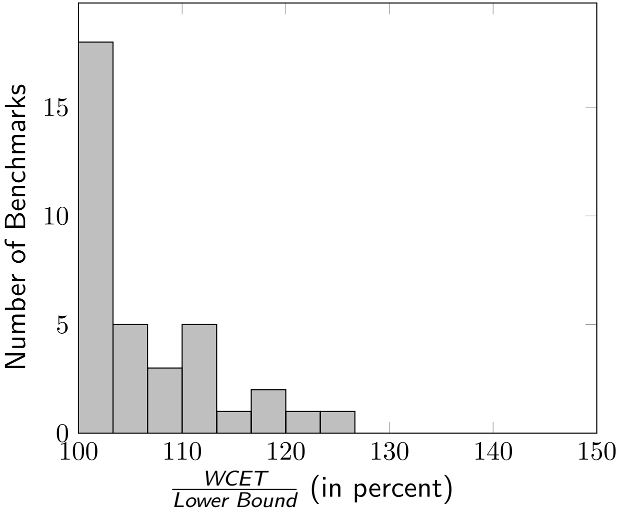
Processor

- ARM(ish) processor with five-stage, in-order pipeline
- Single-level data cache

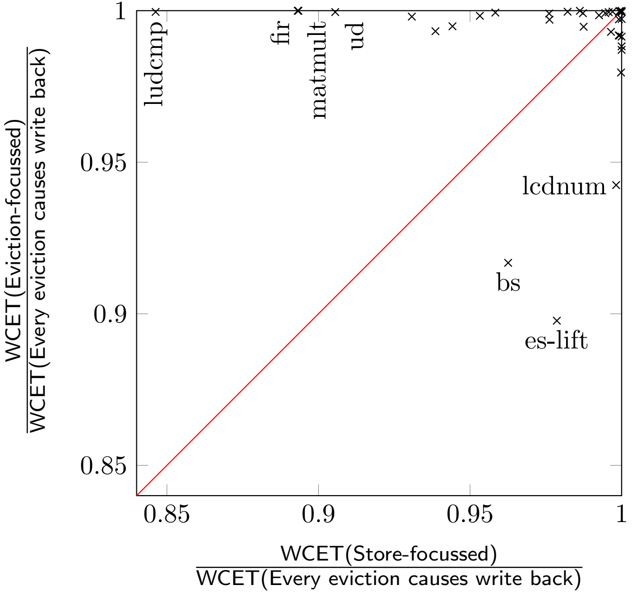
Write back yields lower bounds than write through



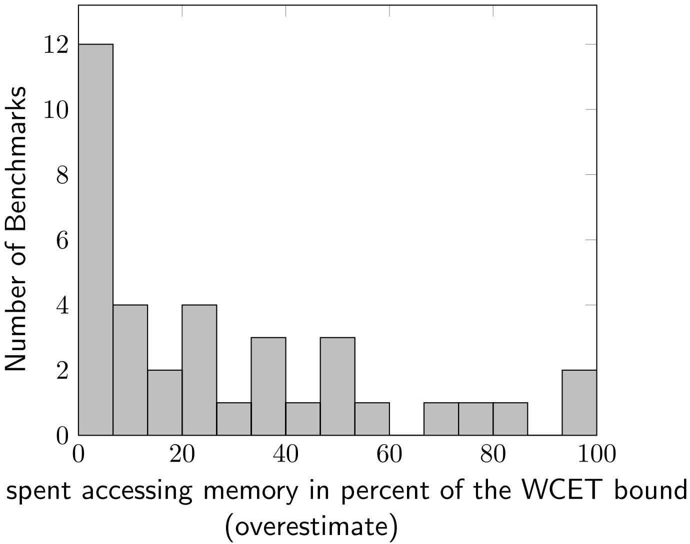
WCET bounds are close to the theoretical lower bound



Eviction-focussed approach is mostly orthogonal to store-focussed approach



Most tasks spend little time accessing memory



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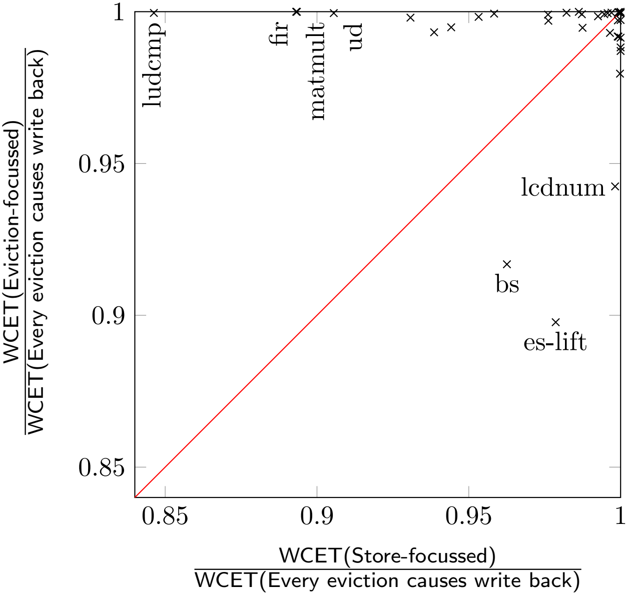

Future Work

- Larger benchmarks
- Integrate into response-time analysis
  (Davis, Altmeyer, Reineke, RTNS 2016)
- Other replacement policies (PLRU, FIFO)

Conclusion

- Write-back caches *are* desirable for hard real-time systems
- Write-back analysis should focus on both, evictions *and* stores

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Thank you very much for your attention!