Verifying the Security of Microarchitectures based on Hardware-Software Contracts

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Joint work with
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Klaus v. Gleissenthall @ VU Amsterdam
Gideon Mohr, Valentin Touzeau @ Saarland University

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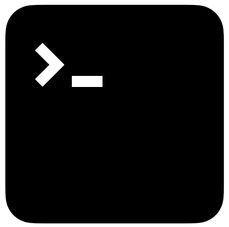
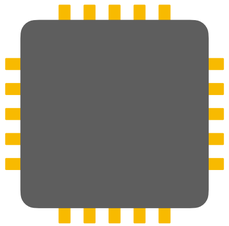
An Introduction to HW/SW Contracts

ISA: Benefits

High-level language



Microarchitecture



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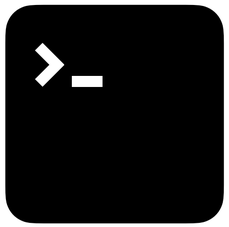
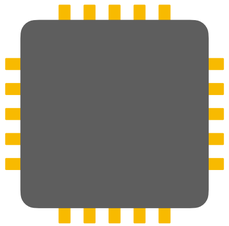


Can program **independently** of microarchitecture

Instruction set architecture (ISA)

Microarchitecture



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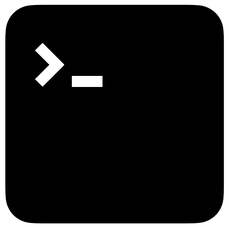

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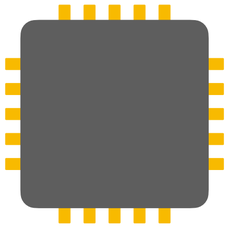
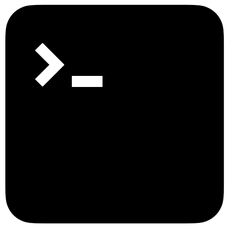


Can program **independently** of microarchitecture

Can implement **arbitrary optimizations** as long as ISA semantics are obeyed

Inadequacy of the ISA: Side channels

High-level language



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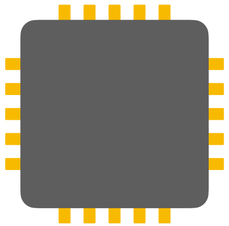

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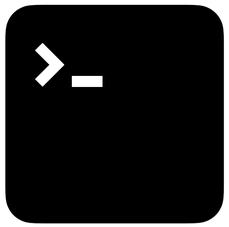

Instruction set architecture (ISA)

No guarantees about side channels

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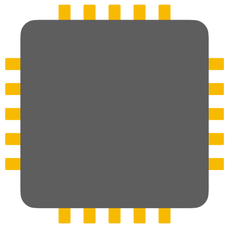

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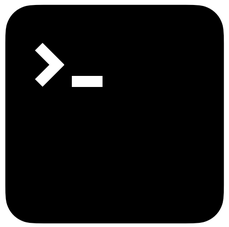

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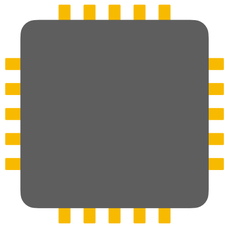

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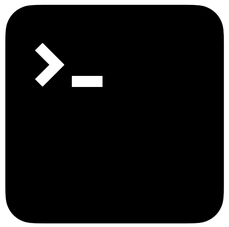

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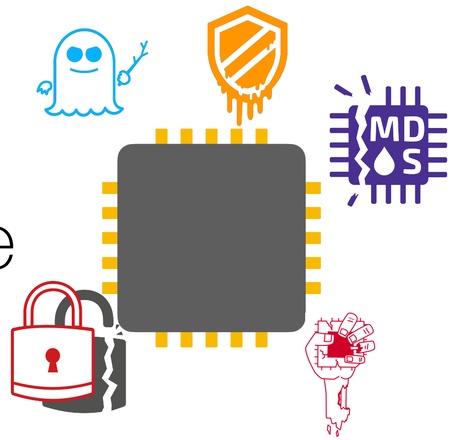

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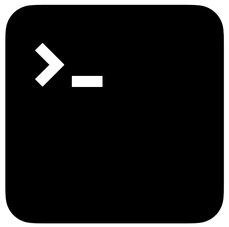

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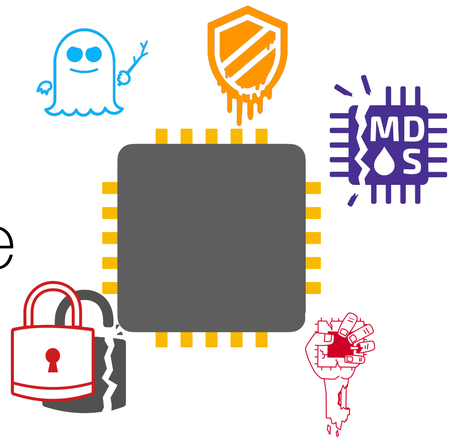

Impossible to program securely
cryptographic algorithms?
sandboxing untrusted code?

No guarantees about side channels

Can implement arbitrary **insecure** optimizations as long as ISA is implemented correctly

A way forward: HW/SW security contracts

HW/SW contract = ISA + X

Succinctly captures
possible information leakage
in a mechanism-independent way

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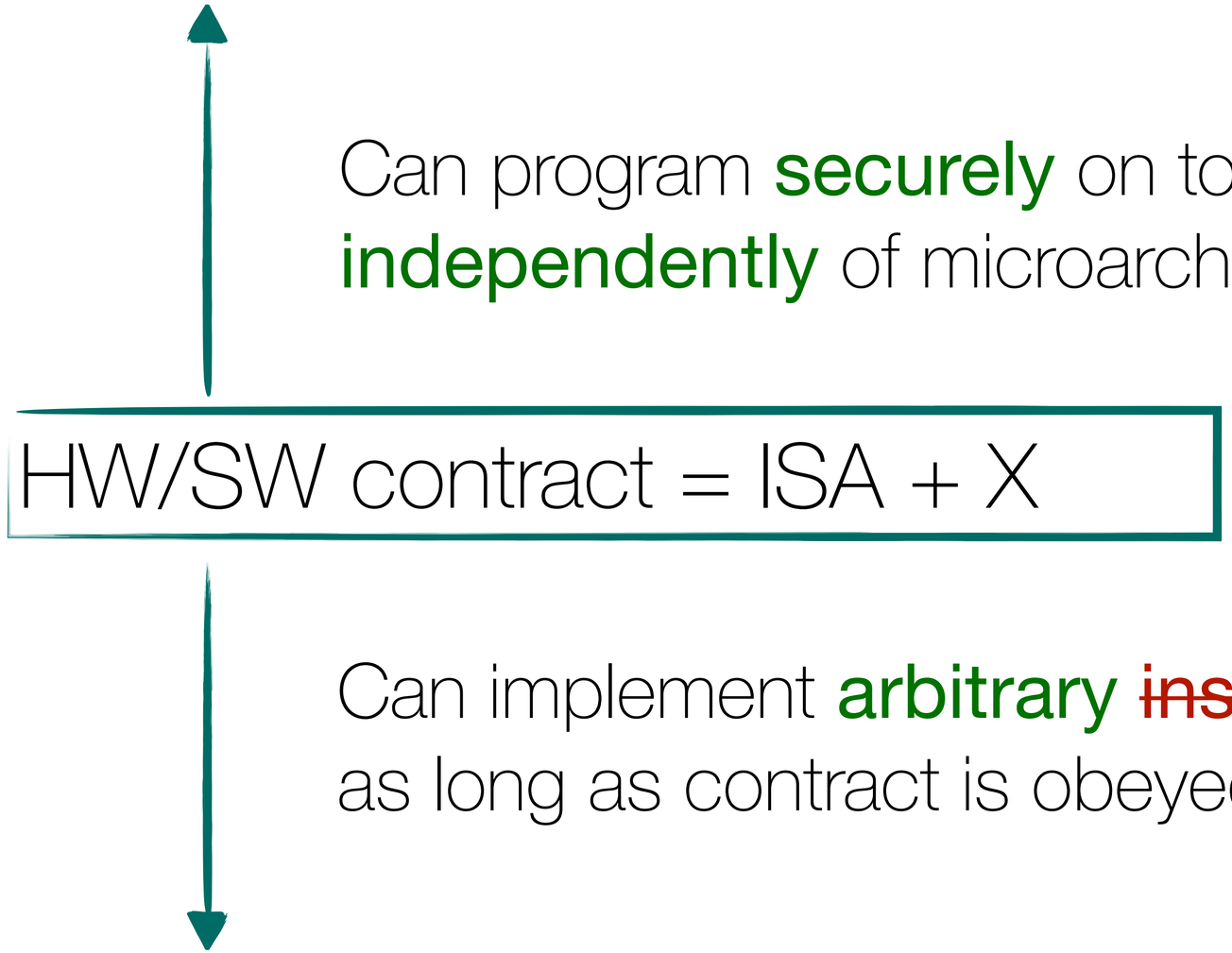

Succinctly captures
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HW/SW contracts

Contracts specify which **program executions**
a side-channel adversary **cannot distinguish**

Contract

ISA

+

Observations

HW/SW contracts

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Captures how
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HW/SW contracts

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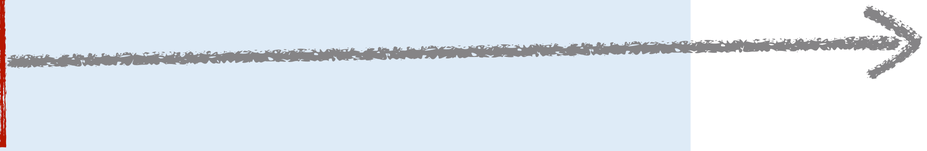
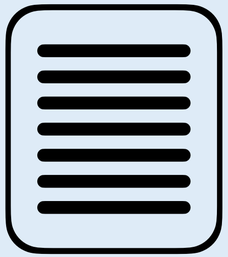


Captures how program is executed

What leaks about an execution

Contracts

Contracts

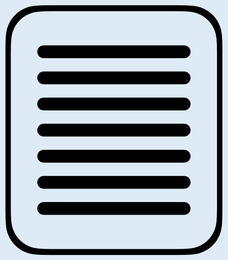


Contract

ISA +

Observations

Contracts



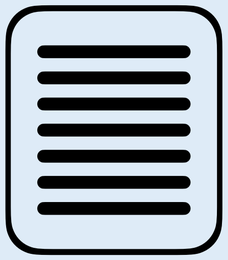
Contract

ISA +

Observations

Contract traces: (p, σ)

Contracts



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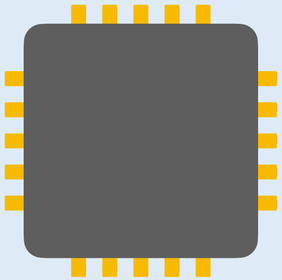
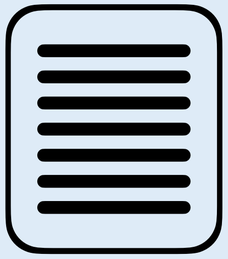


Hardware

µArch design +

Attacker observations

Contracts



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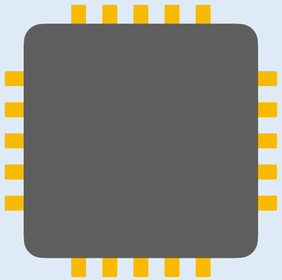

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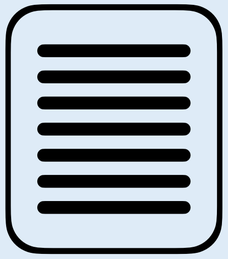

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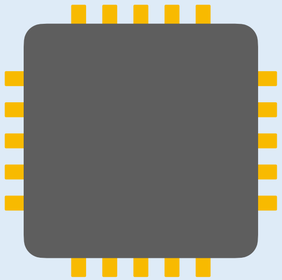

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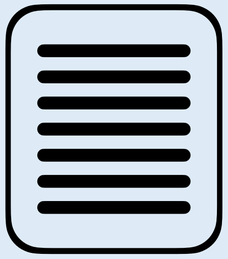

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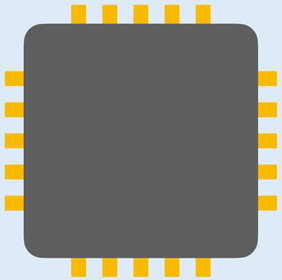

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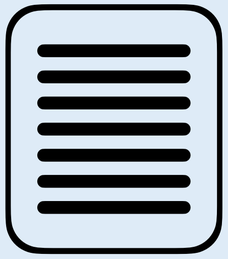

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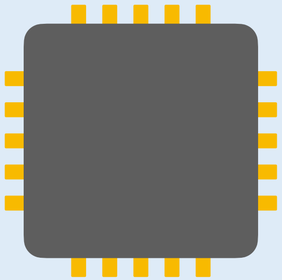

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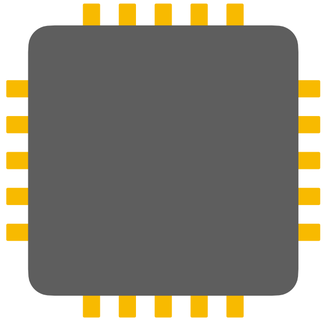
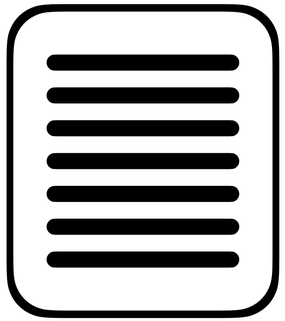
Verifying Contract Satisfaction

Contracts for Real ISAs + Real CPUs



Microarchitecture

$\models$



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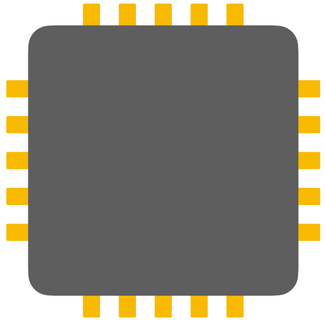
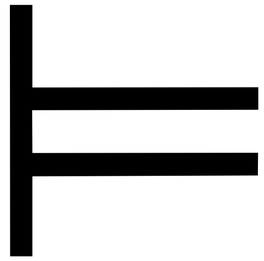
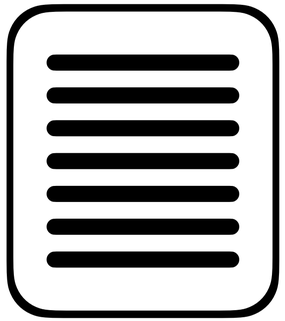
Contracts for Real ISAs + Real CPUs





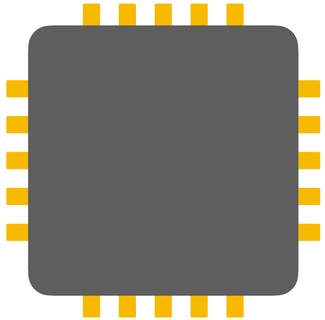


Microarchitecture

Contract

Register transfer level designs

Contracts for Real ISAs + Real CPUs



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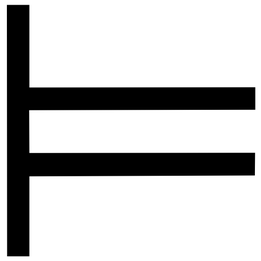
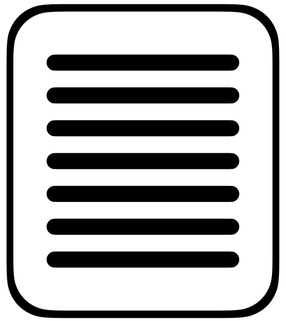


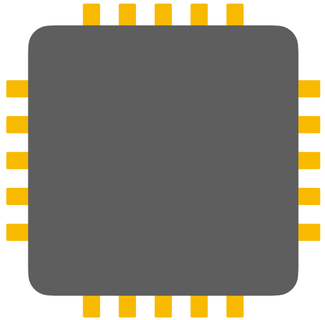


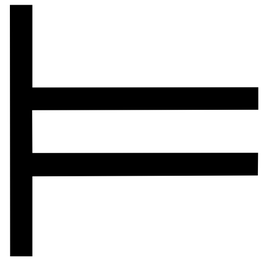
Contract

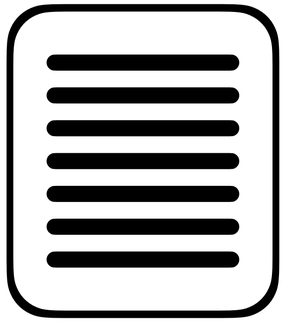
Register transfer level designs

Open-source RISC-V cores

Contracts for Real ISAs + Real CPUs







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ISA spec.
+ Observations

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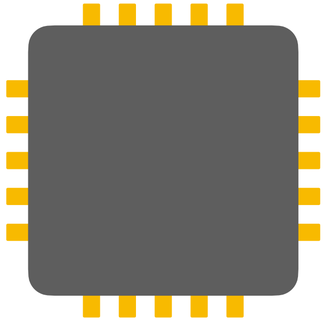

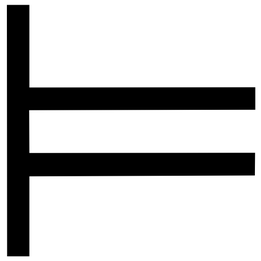

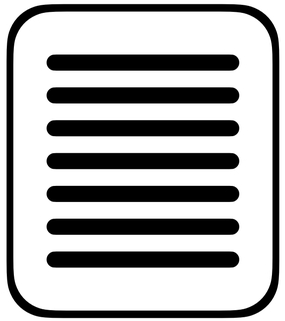

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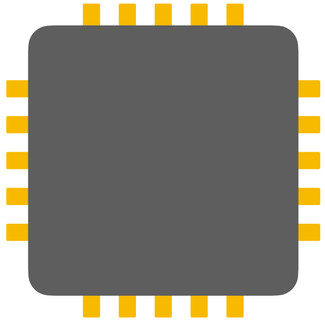

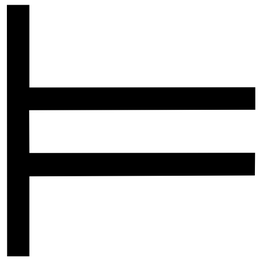

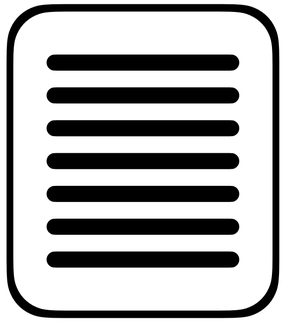

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Open-source RISC-V cores

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ISA spec. + Observations

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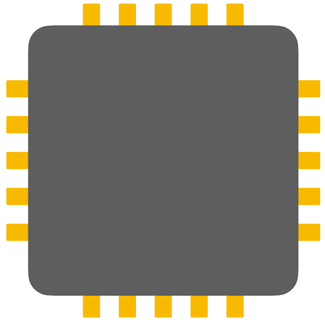
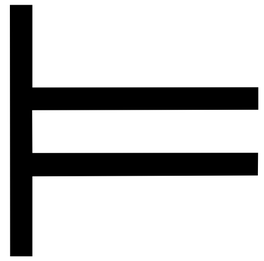
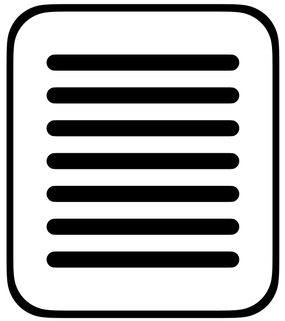
2. Single-cycle RISC-V reference implementation + Combinatorial observer

Contracts for Real ISAs + Real CPUs







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Automatic proof

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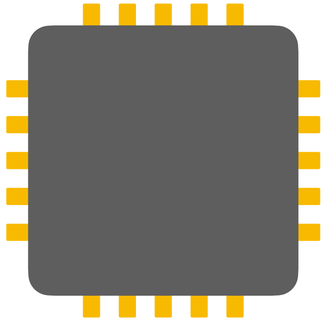
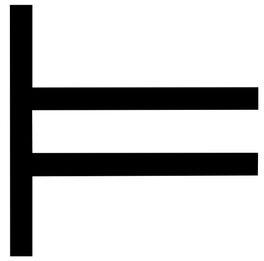
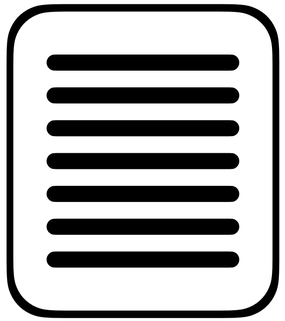
Contracts for Real ISAs + Real CPUs







Microarchitecture

Contract

Register transfer level designs

Automatic proof

ISA spec.
+ Observations

Open-source RISC-V cores

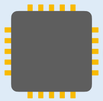
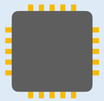
SMT solvers + Invariant inference

1. Sail (https://github.com/rems-project/sail)

2. Single-cycle RISC-V reference implementation + Combinatorial observer

Verification: 4-way product circuit + Induction

Contract satisfaction

Hardware  satisfies contract  if for all programs p and arch. states σ, σ': if  $(p, \sigma) =$  (p, σ') then  $(p, \sigma) =$  (p, σ')

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Hardware 🔲 satisfies contract 📄 if for all programs p and arch. states σ, σ': if 📄$(p, \sigma) =$ 📄(p, σ') then 🔲$(p, \sigma) =$ 🔲(p, σ')

ISA_1

$\approx_{ISA}$

HW_1

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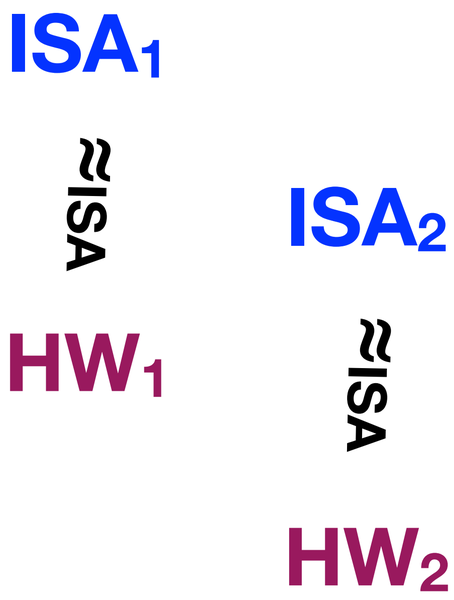

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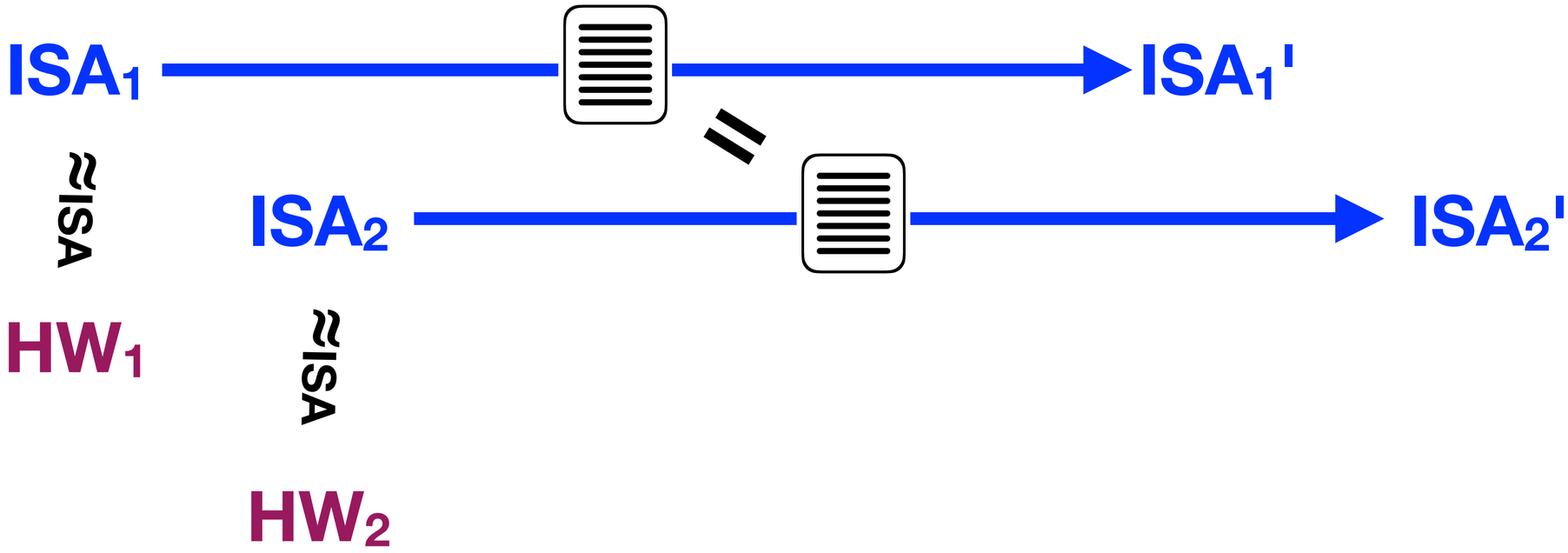

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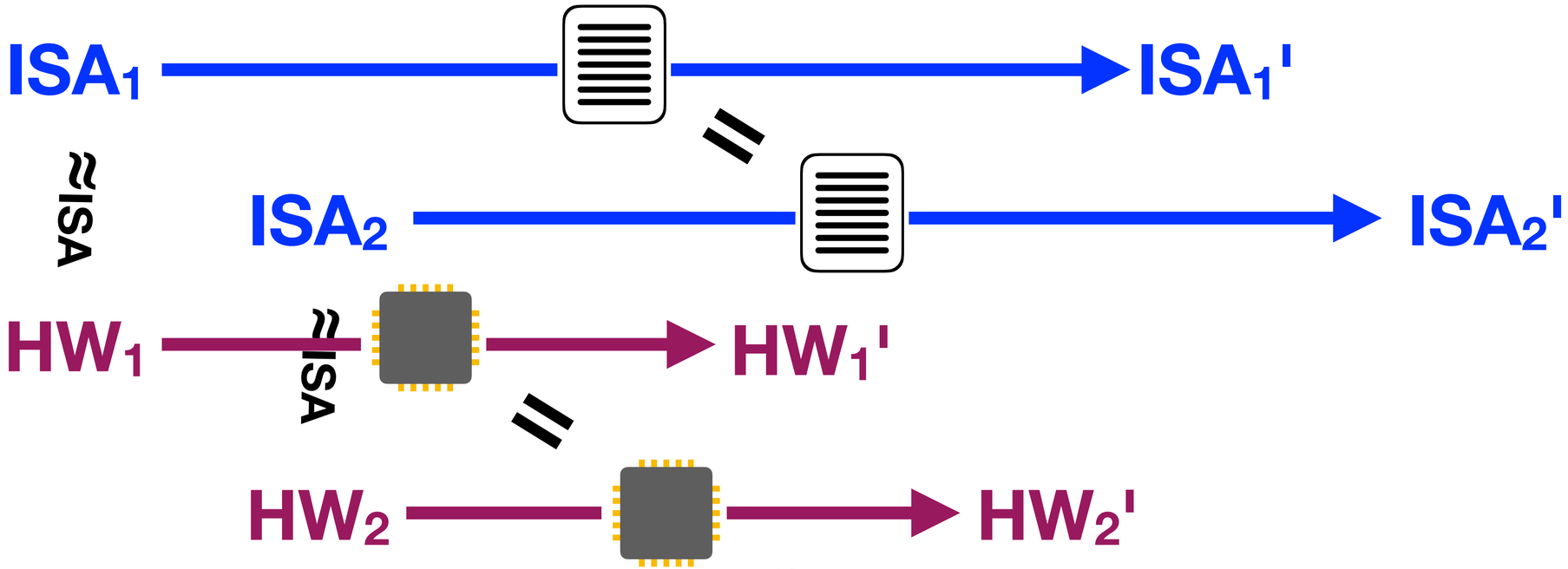

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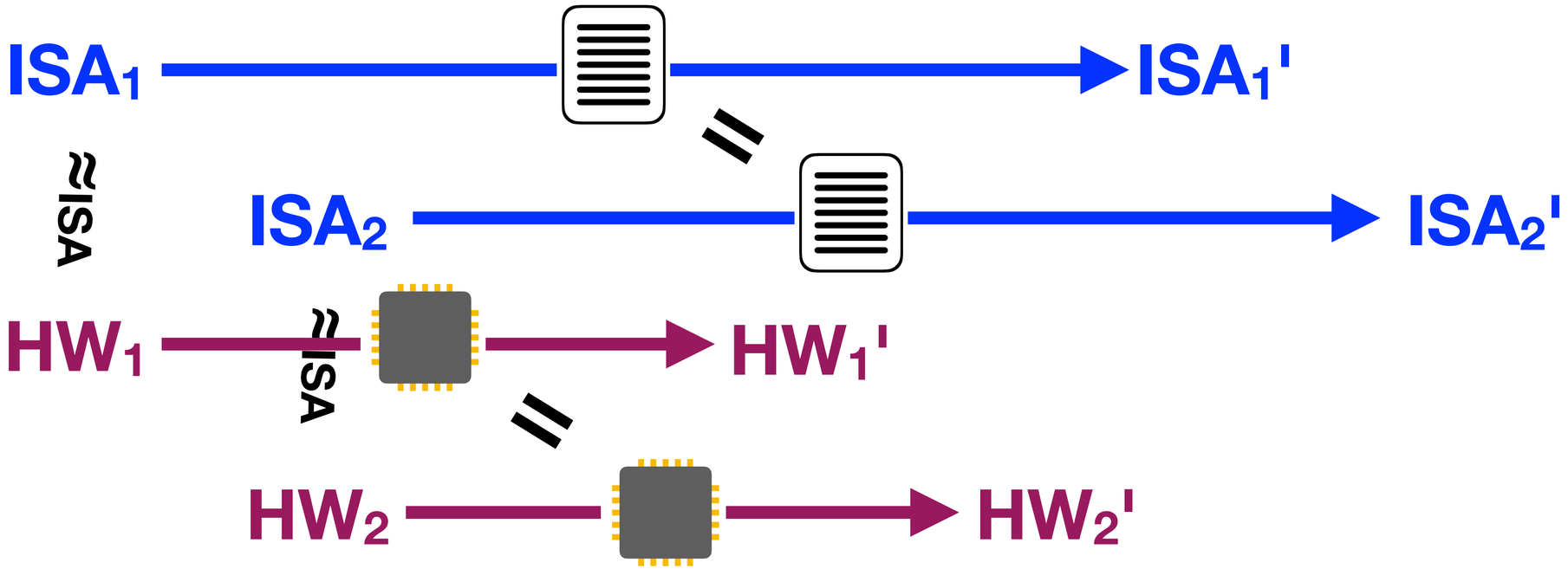

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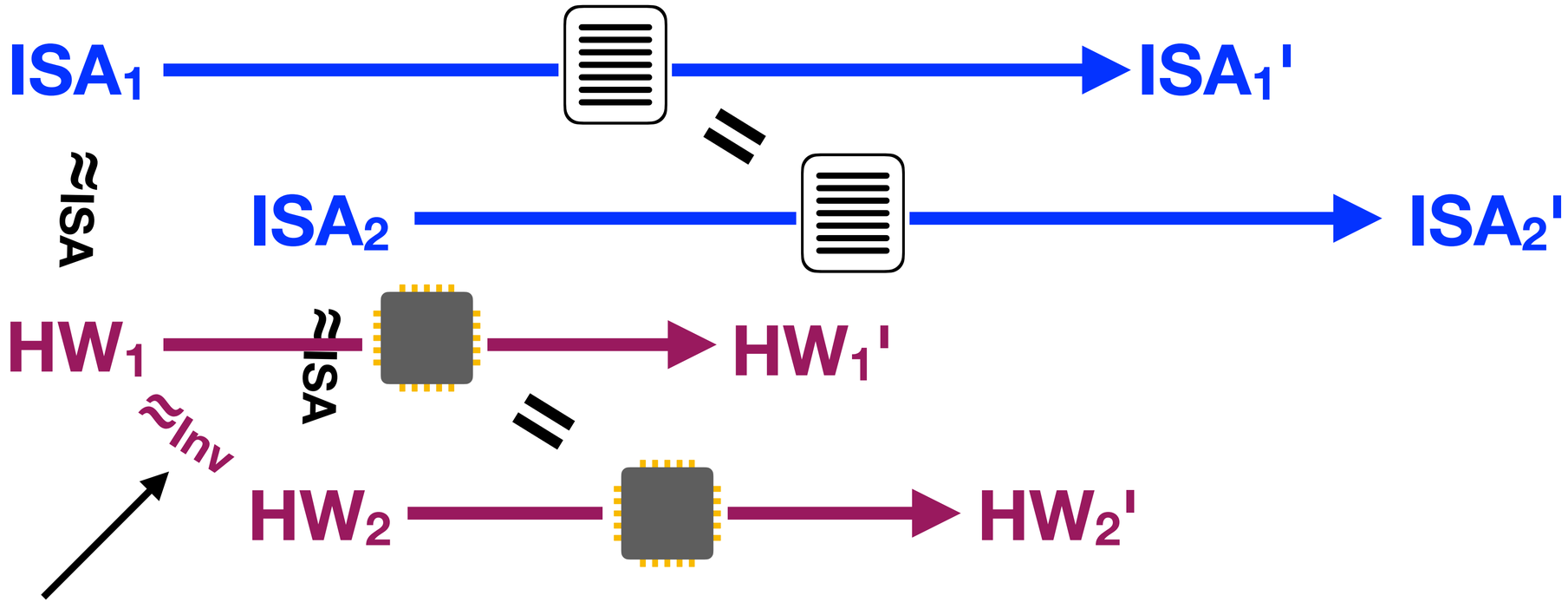
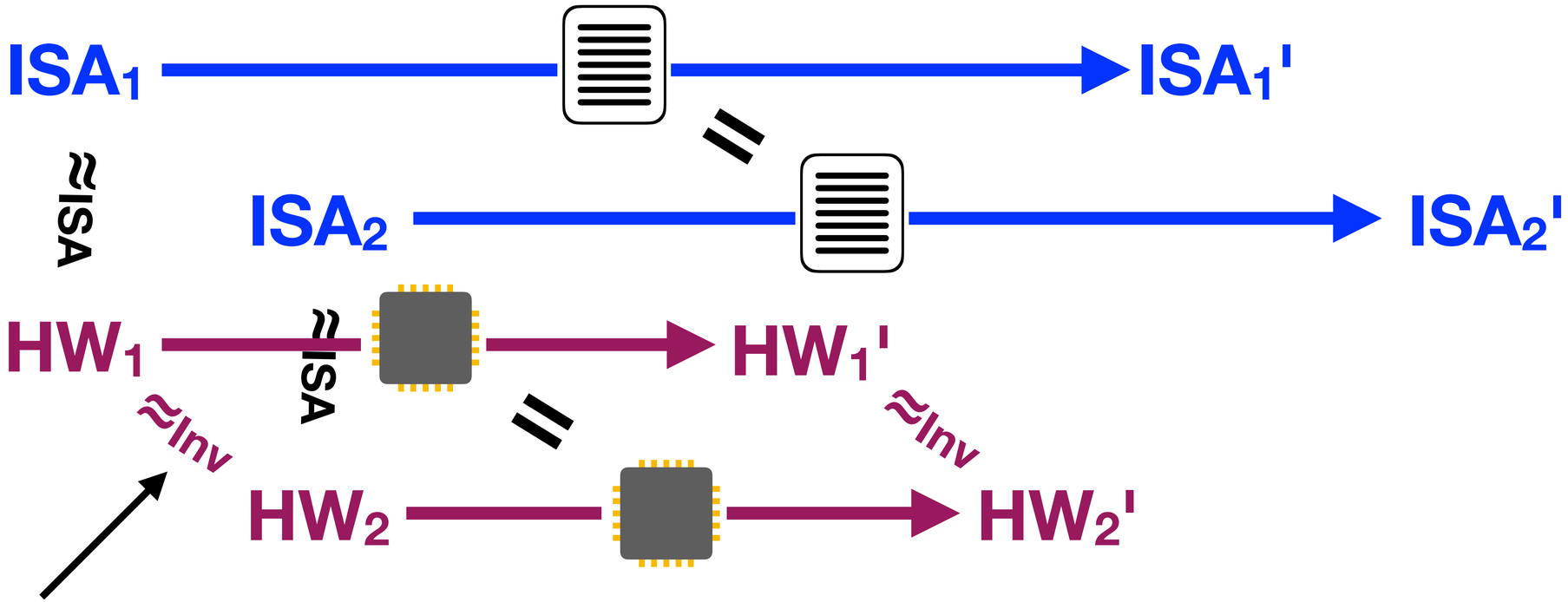


Relational
Inductive
Invariant

Verification: 4-way product circuit + Induction



Relational Inductive Invariant

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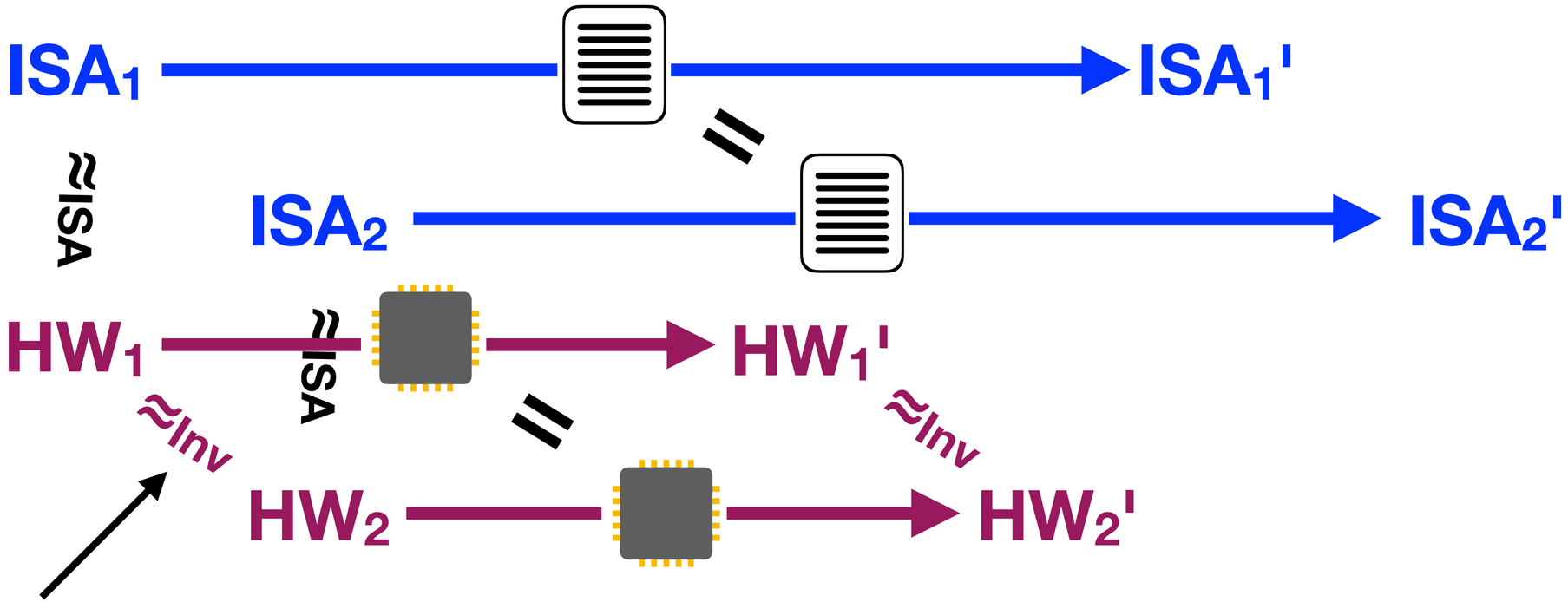

Relational Inductive Invariant

... synthesized using Houdini algorithm

(Flanagan+Leino: Houdini, an Annotation Assistant for ESC/Java, Formal Methods Europe)

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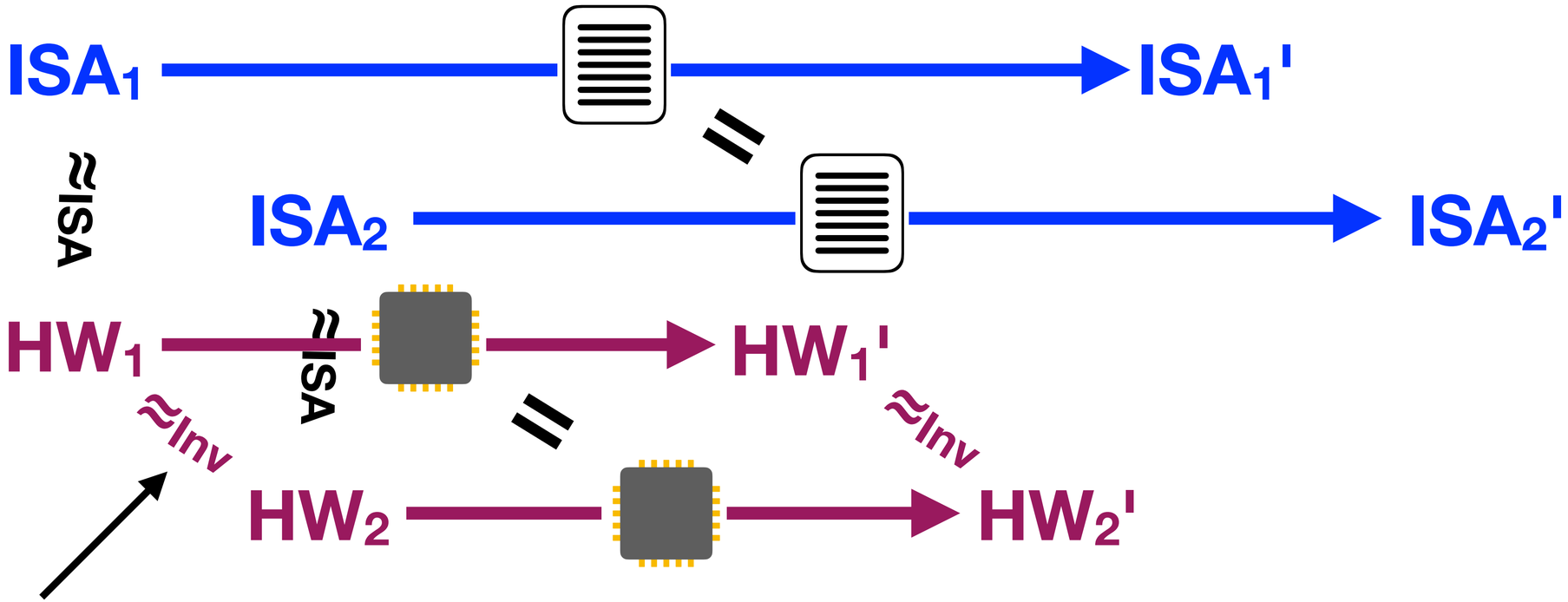

Relational Inductive Invariant

Works on small examples.
RISC-V Sodor Work-in-progress

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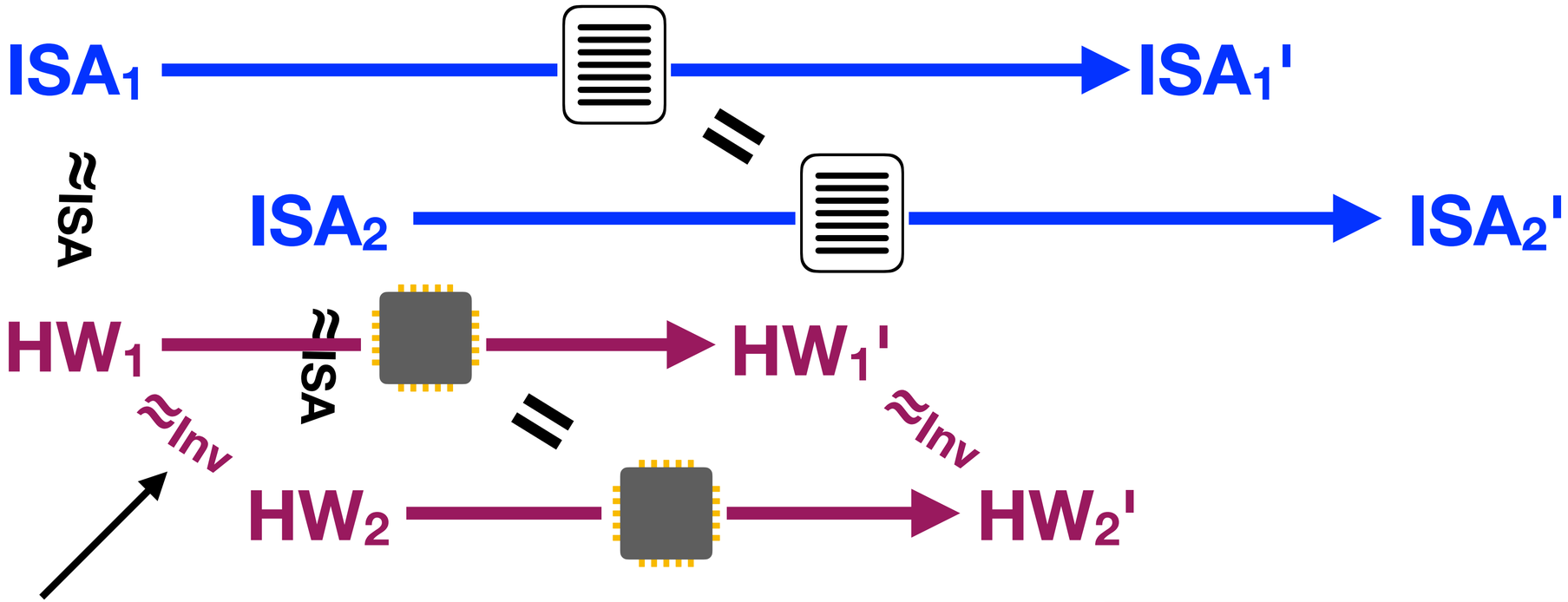

Relational Inductive Invariant

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Scalability limited due to 4-way product circuit

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Disentangling Leakage and ISA satisfaction

Contract satisfaction

Hardware satisfies contract if for all programs p and states σ, σ':

if $Obs(ISA)(p, \sigma) = Obs(ISA)(p, \sigma')$

then $Atk(\mu Arch)(p, \sigma) = Atk(\mu Arch)(p, \sigma')$

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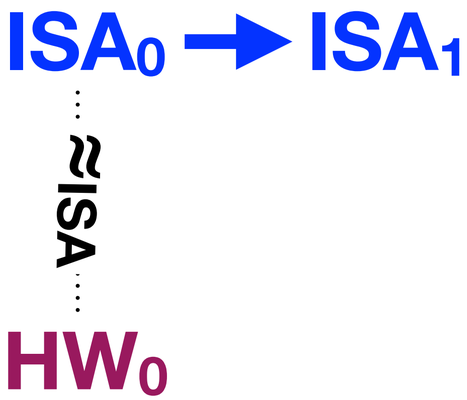
ISA satisfaction + **Leakage satisfaction**

ISA satisfaction

ISA satisfaction



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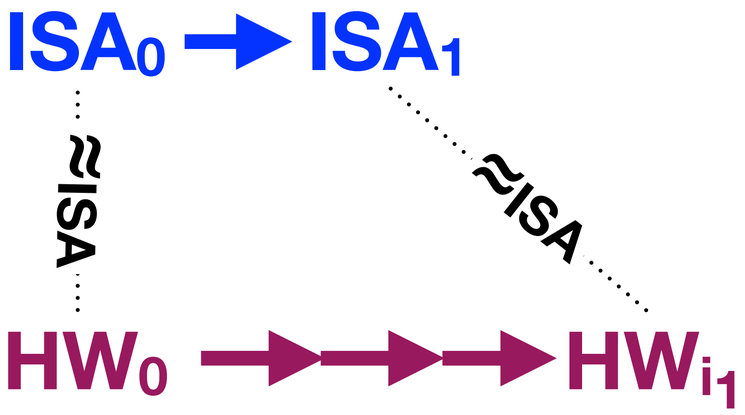

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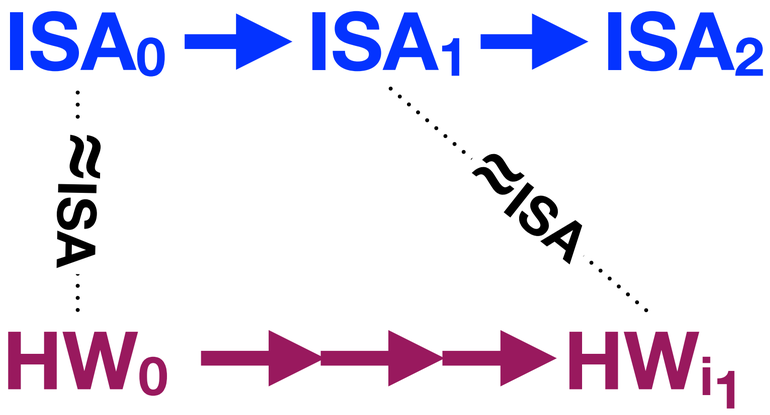

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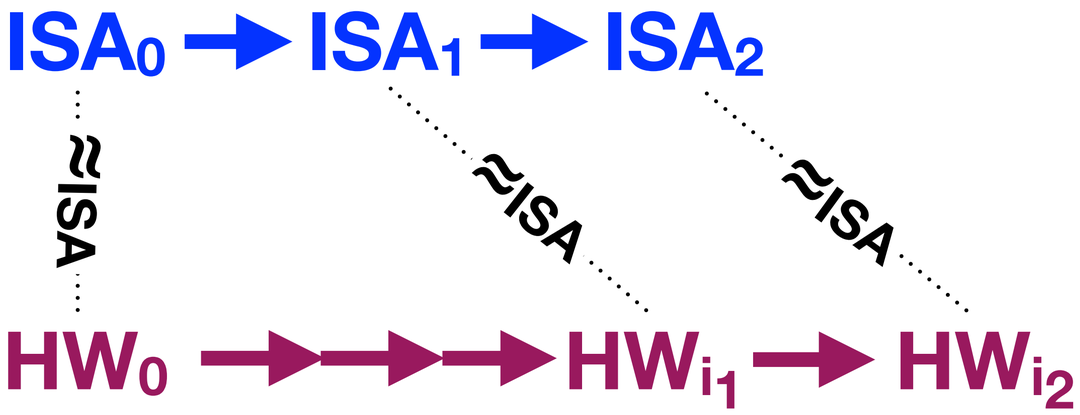

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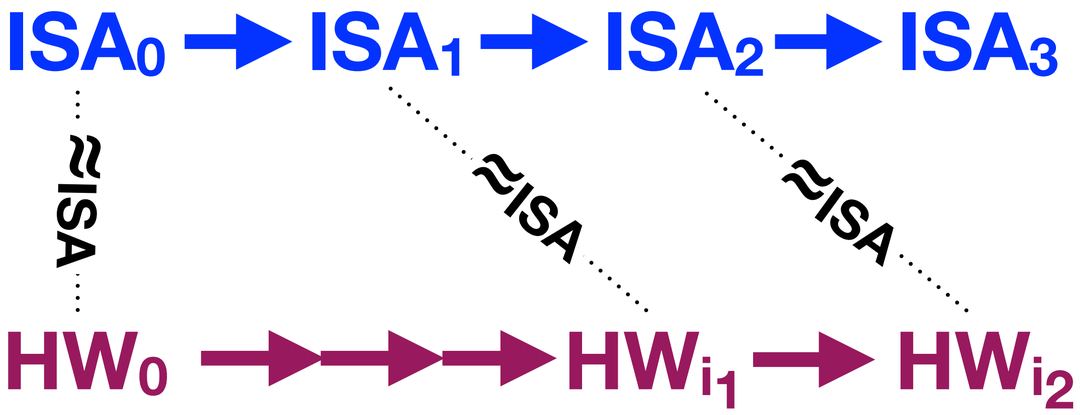

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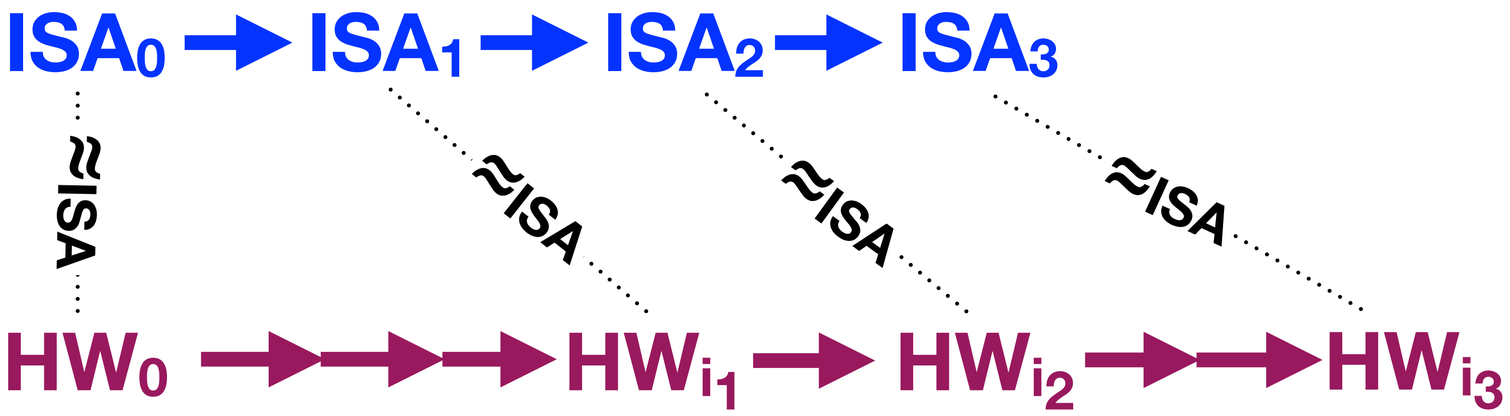

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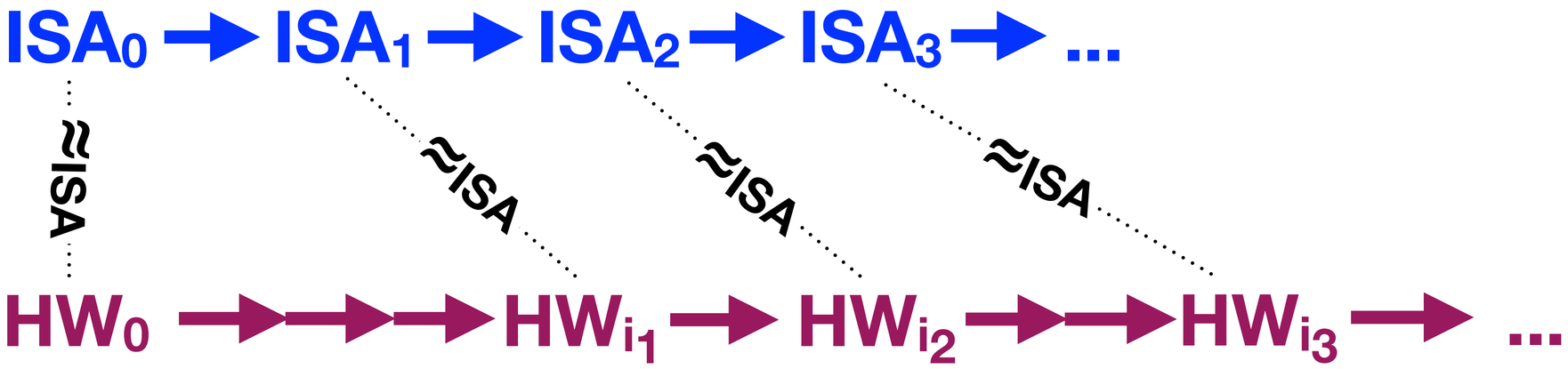

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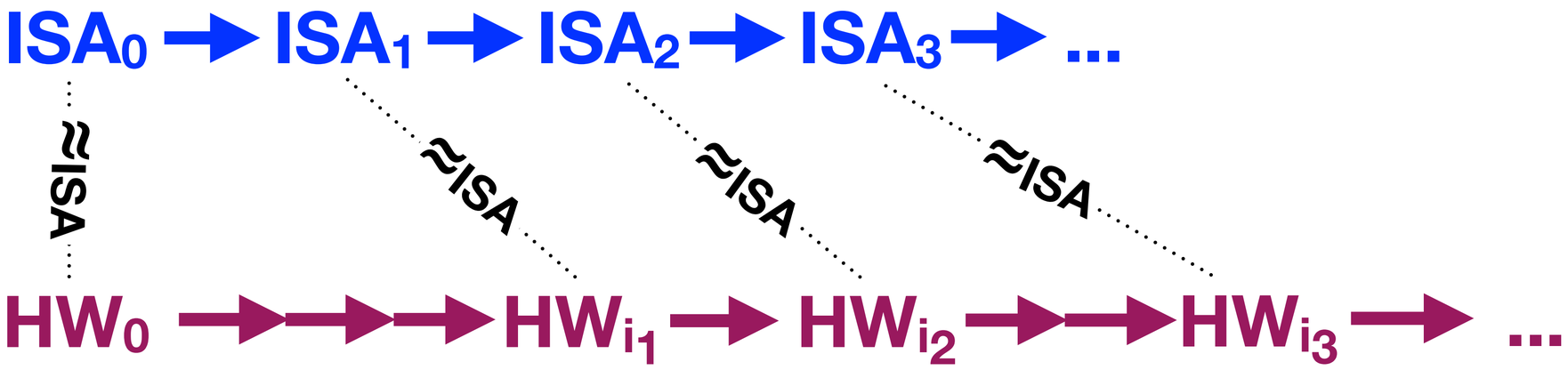

The ISA trace is embedded in the HW trace.

Leakage satisfaction

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+ Observations determine the timing of instruction retirement.

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Verified DarkRISCV leakage

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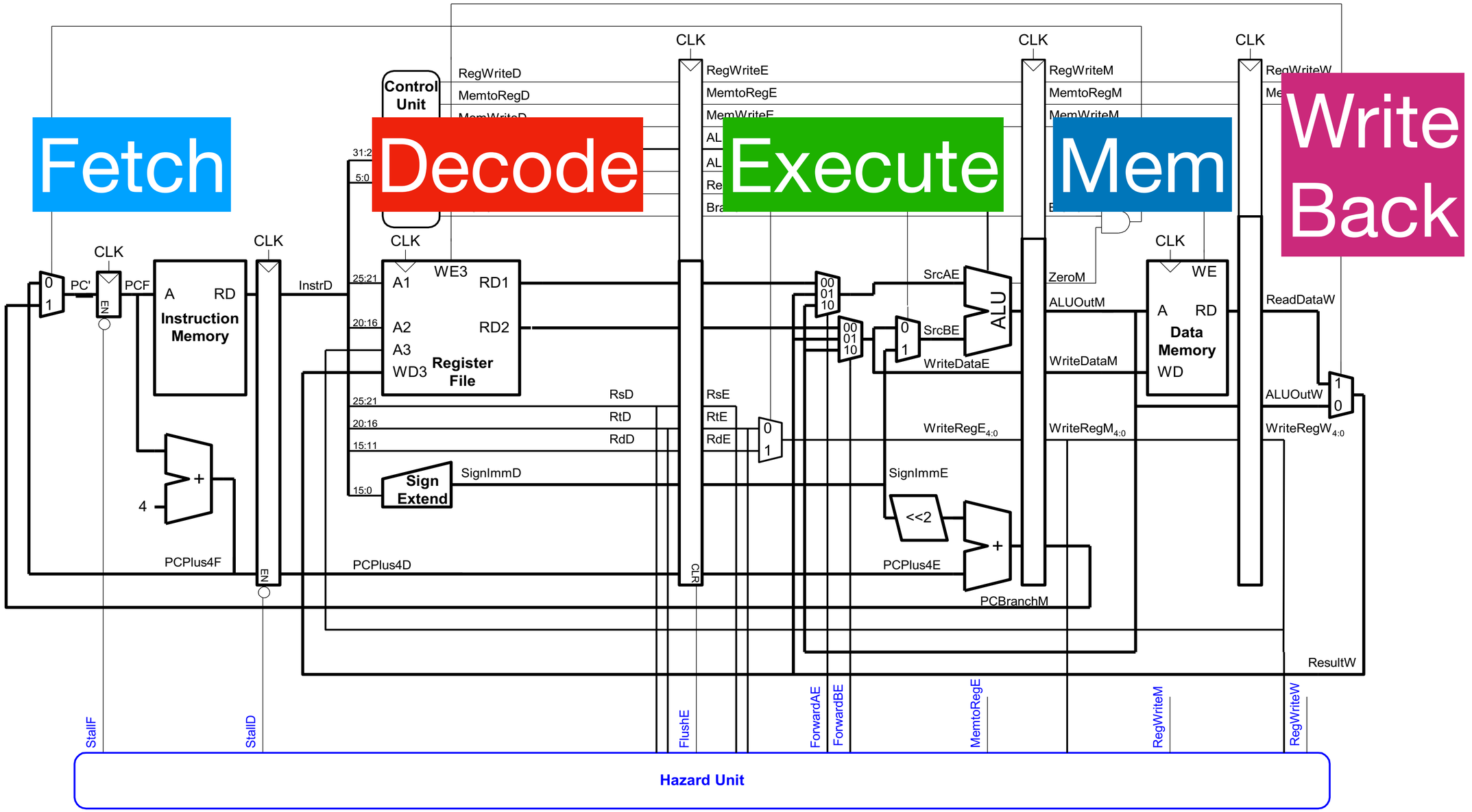
Verified DarkRISCV leakage

Proof relies on "pipeline invariants"

Pipeline invariants: Example



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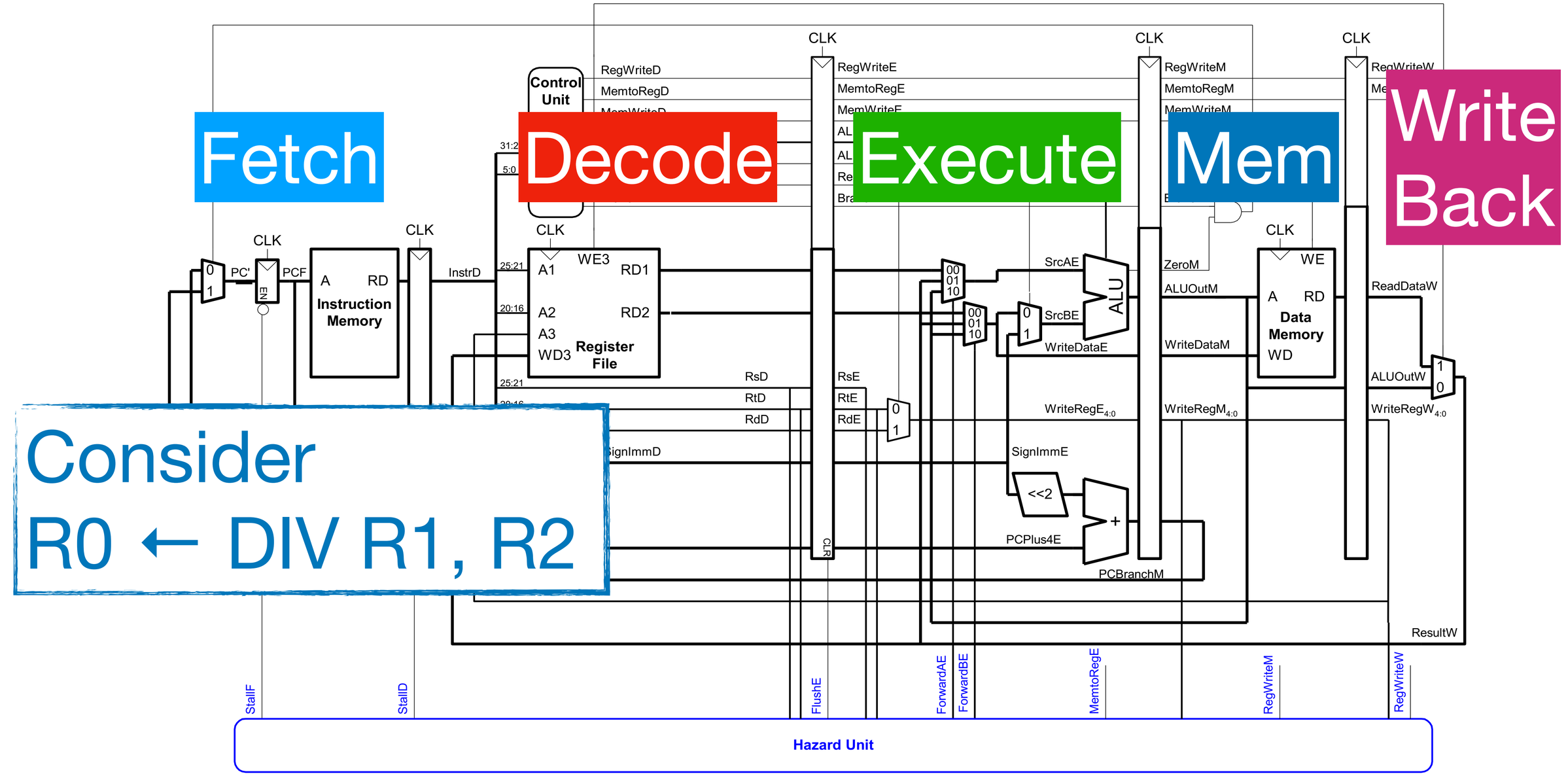

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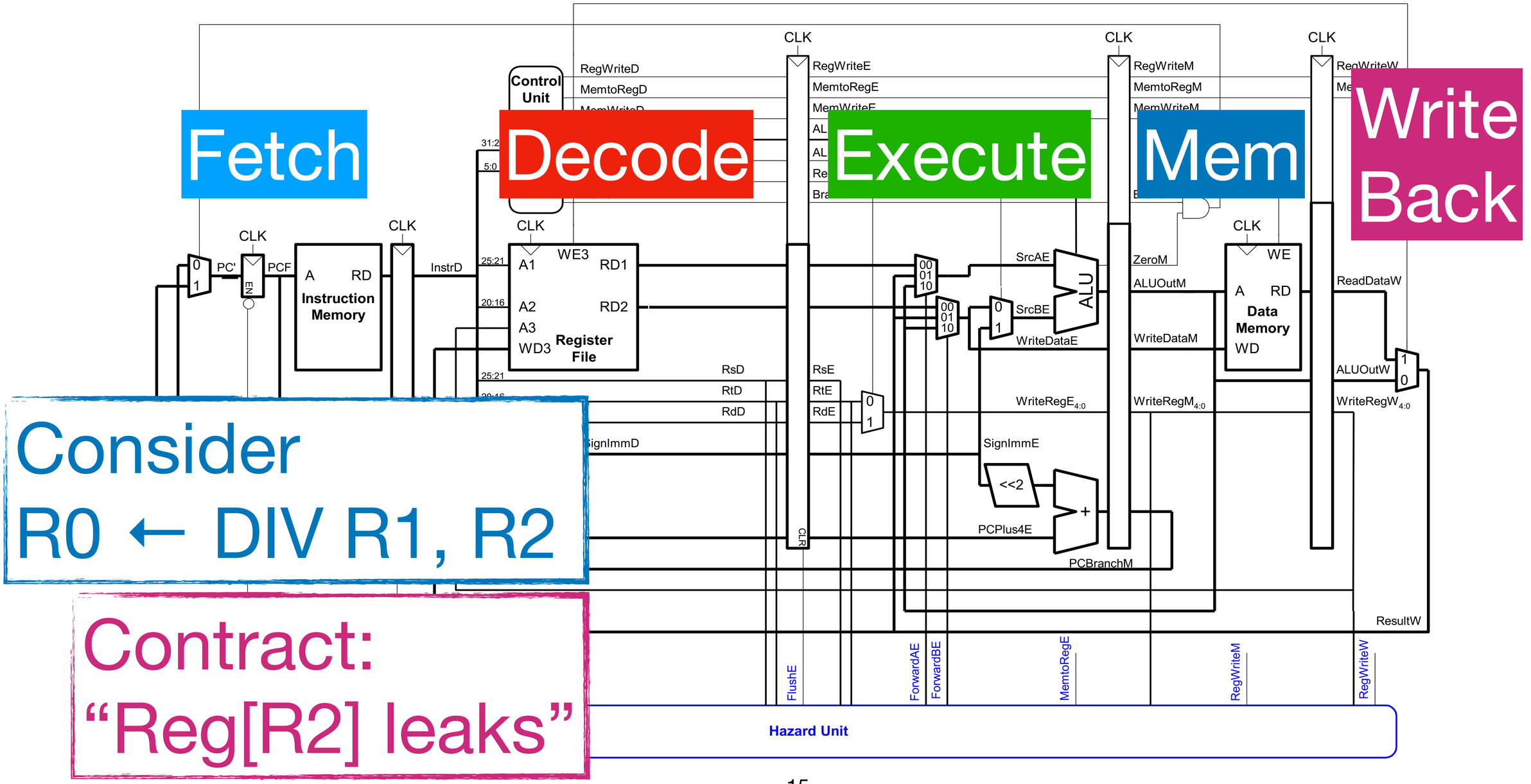
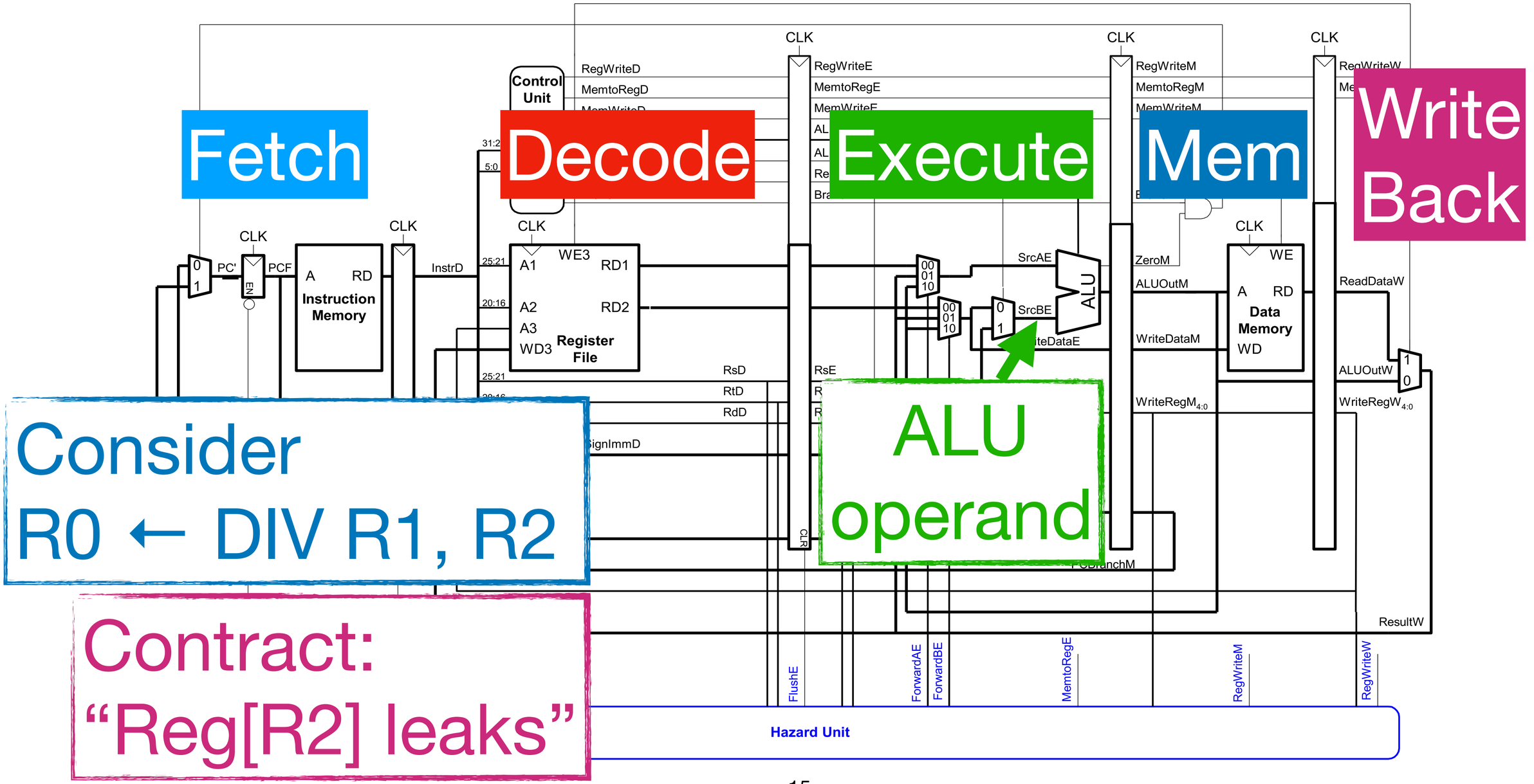


Consider
R0 ← DIV R1, R2

Contract:
“Reg[R2] leaks”

Pipeline invariants: Example



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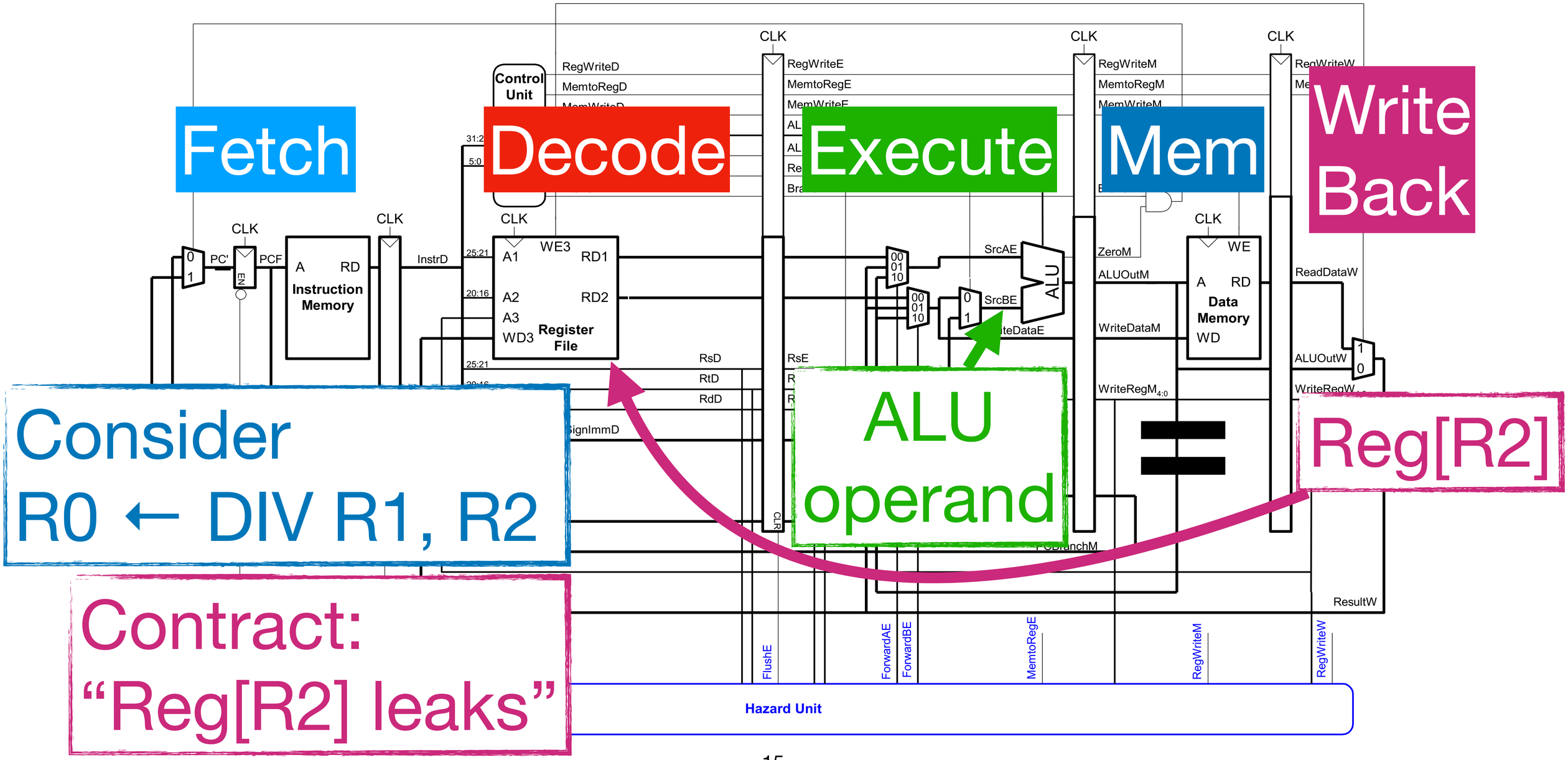

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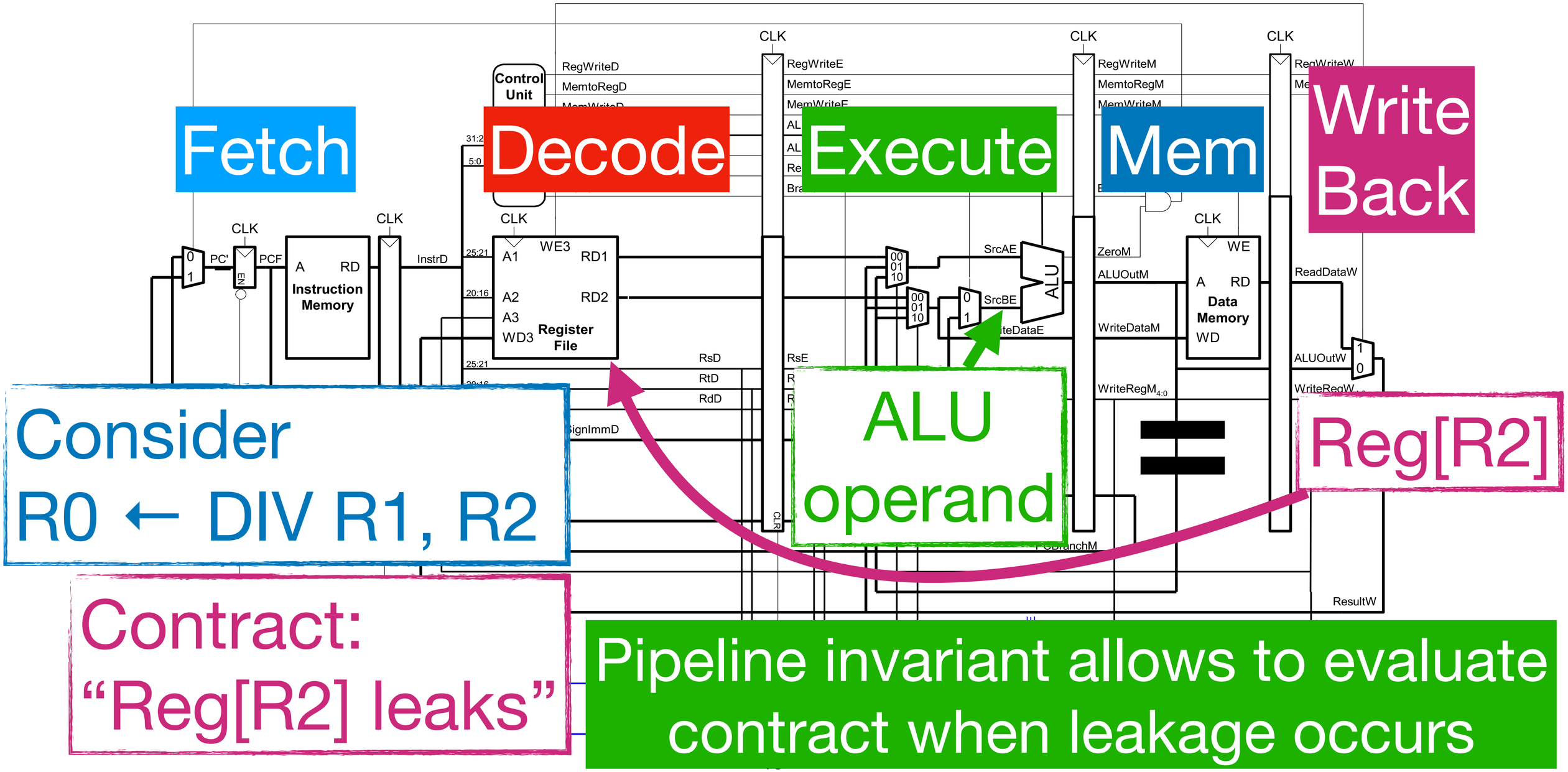

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Come to our poster to discuss!