Selfish-LRU:

Preemption-Aware Caching for *Predictability* and *Performance*

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Context: Preemptive Scheduling

Non-preemptive Execution:

Task 1

Task 2

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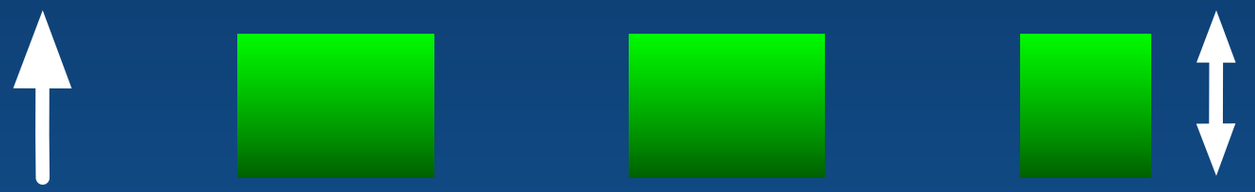
Preemptive Execution:

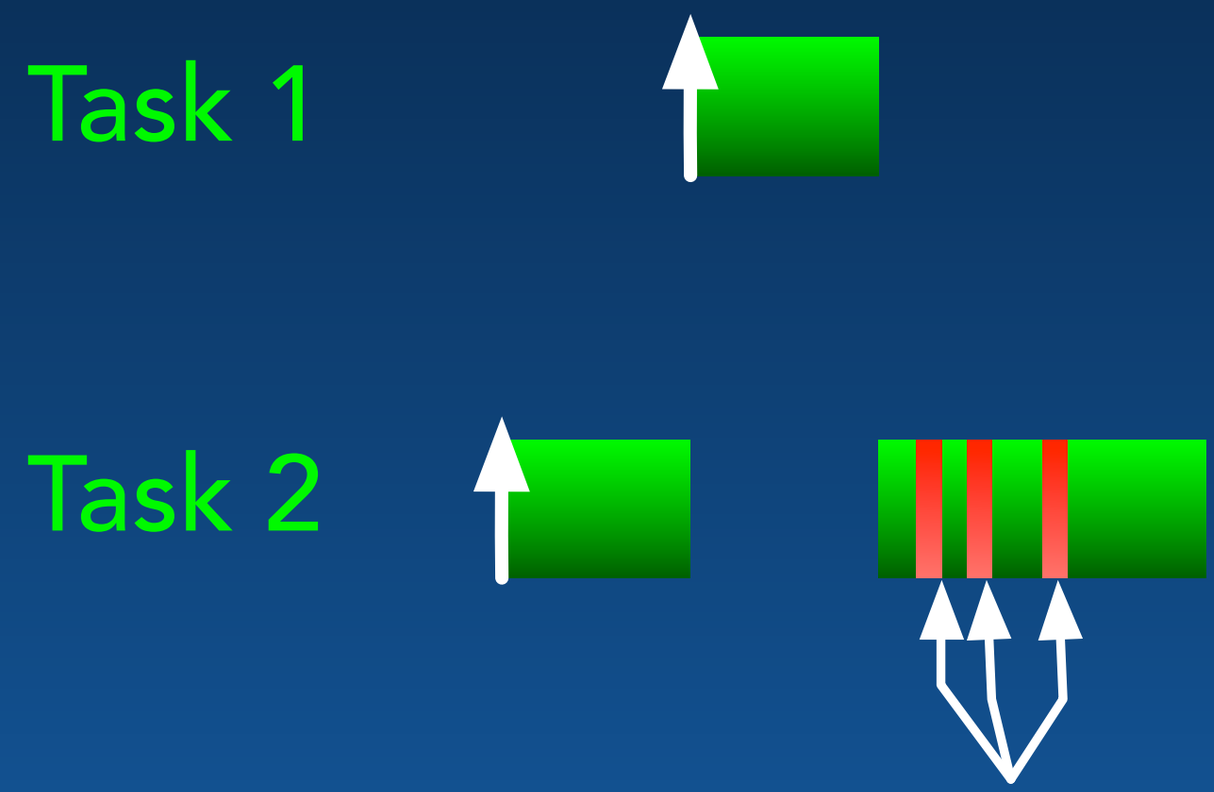
Task 1

Task 2



Caveat: Preemptions are **not** free!

Preemptive Execution:



Cache-Related Preemption Delay (CRPD)

Contribution of this paper

Selfish-LRU: a new cache replacement policy, that

➡ Increases performance by *reducing* the CRPD

➡ *Simplifies* static analysis of the CRPD

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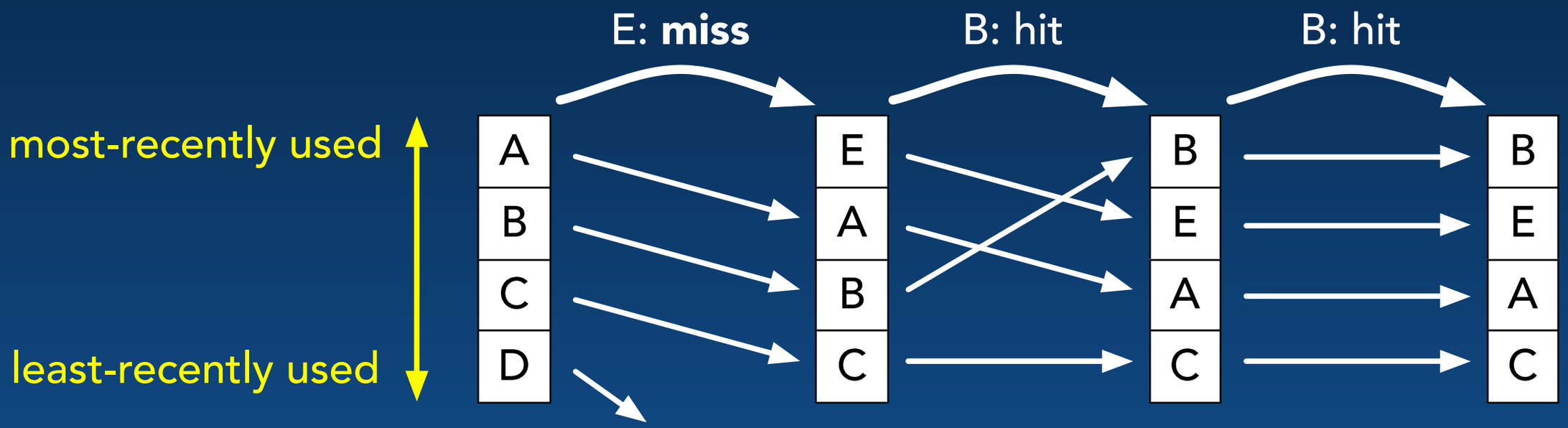
Selfish-LRU is a *preemption-aware* variant of *least-recently used* (LRU)

Least-Recently Used (LRU)

"Replace data that has not been used for the longest time"



➡ Usually works well due to temporal locality

CRPD Example under LRU Replacement

Assume simple **preempted** task:

```
for i in [1,10]:
     do something()
```

```
for i in [1,10]:
     access A
     access B
     access C
     access D
```

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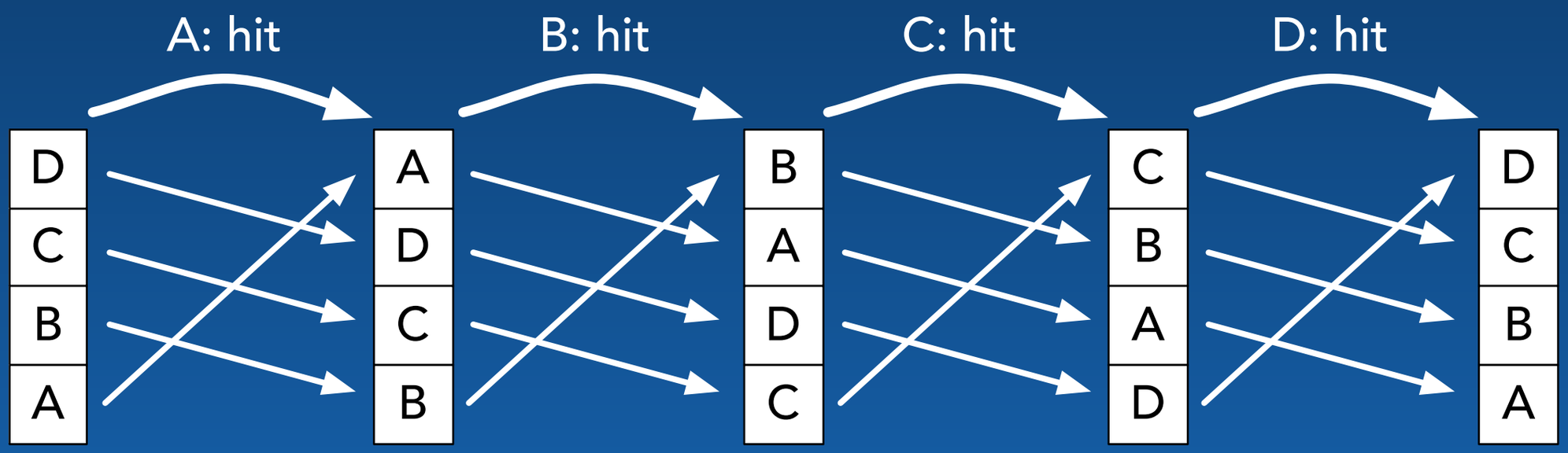
Without preemption (after warmup): **0 misses**



CRPD Example under LRU Replacement

Assume simple **preempting** task:

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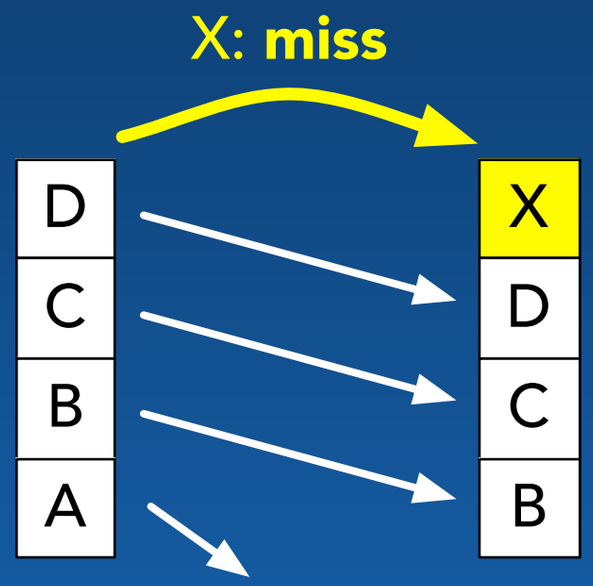
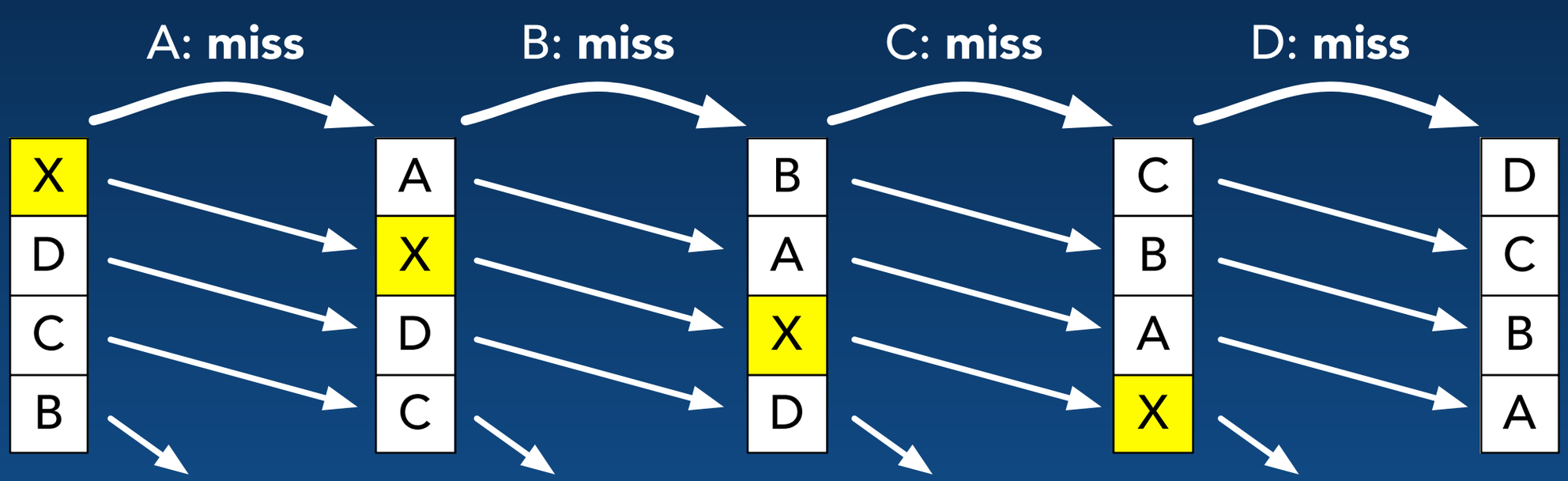
do something_else()  →  access X
```

Preemption between loop iterations: 1 access



CRPD Example under LRU Replacement

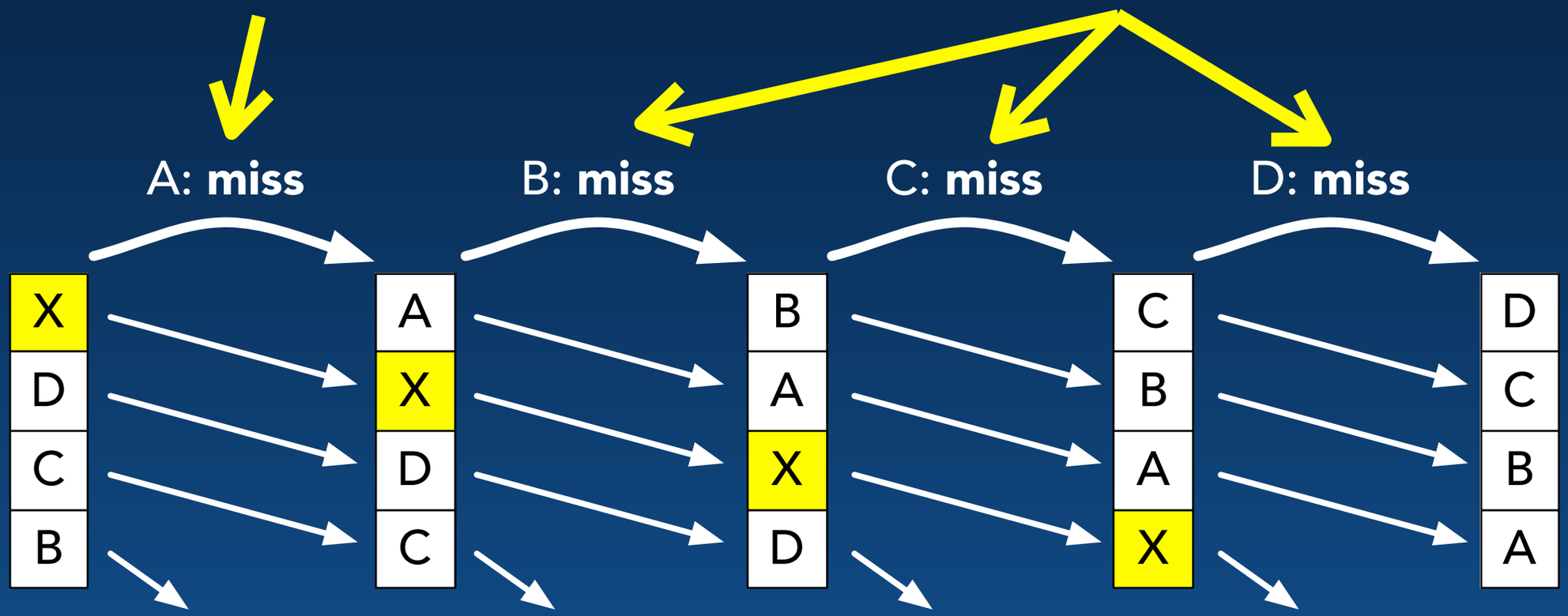
First loop iteration after preemption: **4 misses**



CRPD Example under LRU Replacement:
Two types of misses related to preemption

1. Replaced Misses

2. Reordered Misses



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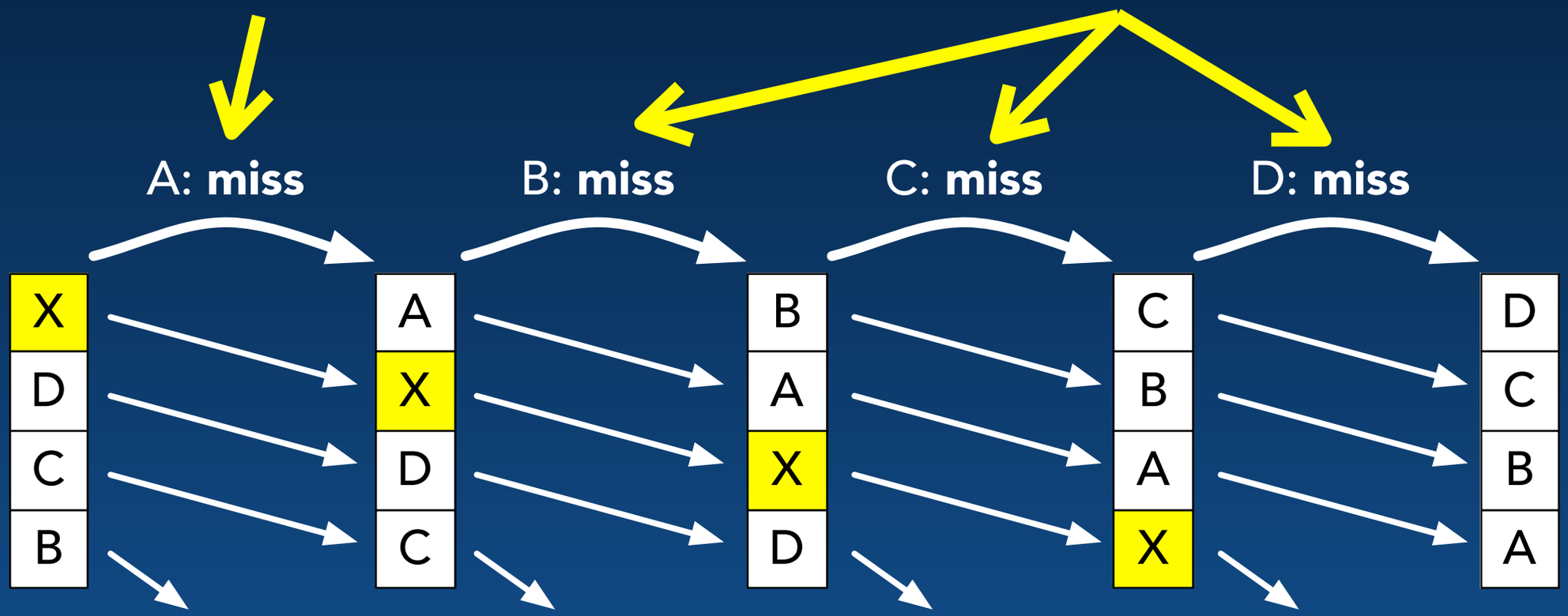
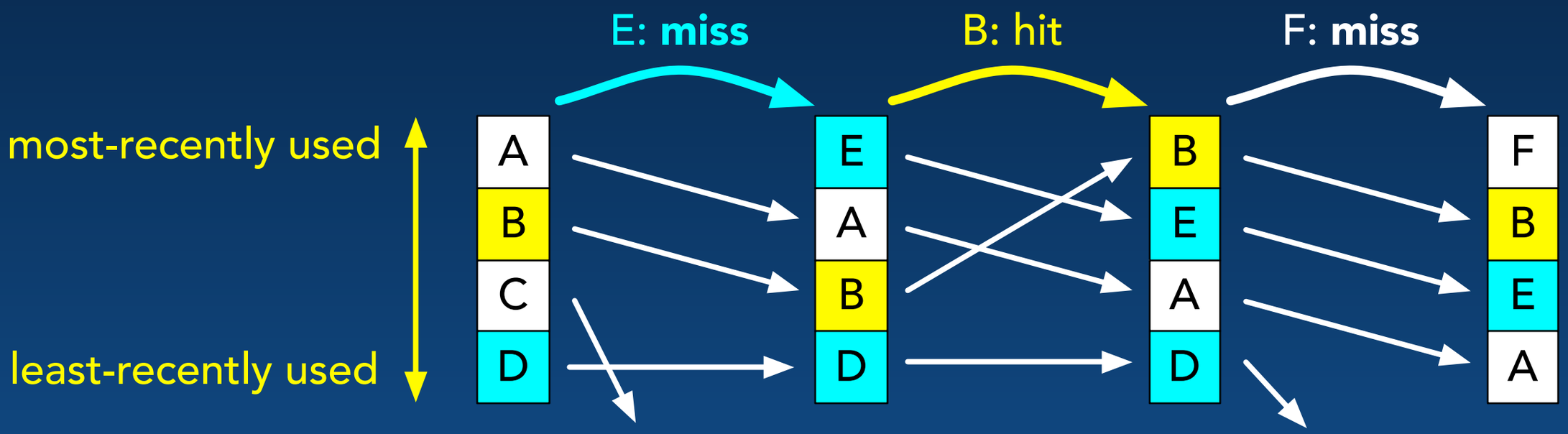


Liu et al., PACT 2008: reordered misses account for **10%** to **28%** of all preemption-related misses

Selfish-LRU: Idea

Prioritize blocks of currently running task:



Intuition:
"Memory blocks of currently running task more likely to be accessed again soon."

Selfish-LRU: CRPD Example Revisited

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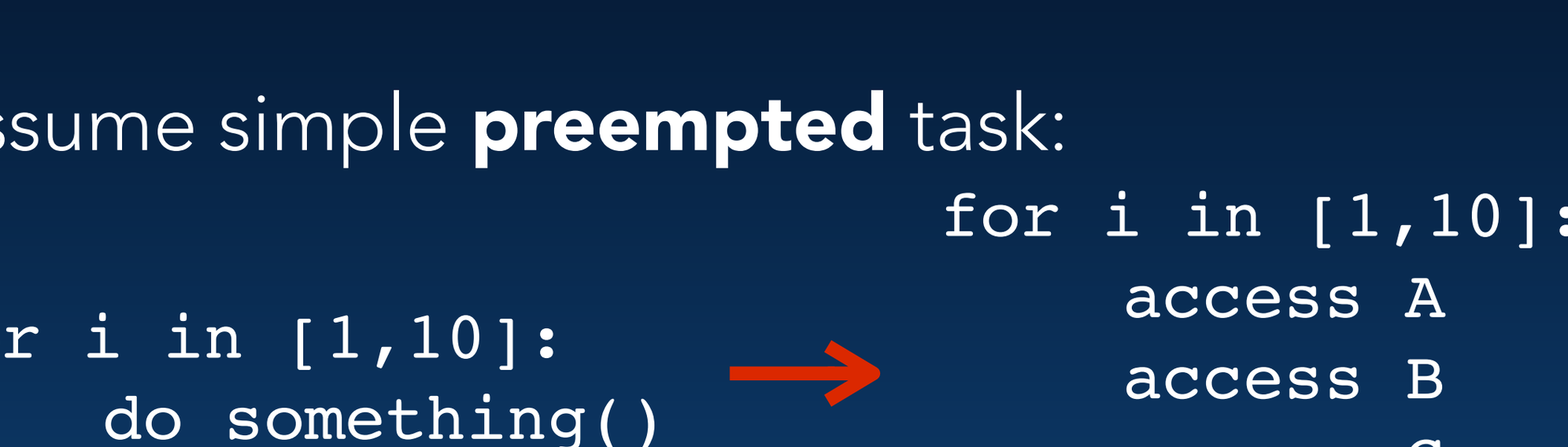

➡ Same behavior as LRU

Selfish-LRU: CRPD Example Revisited

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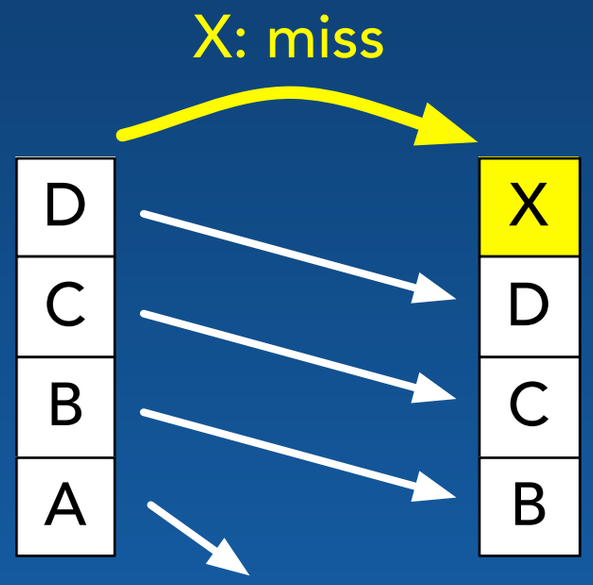

Selfish-LRU: CRPD Example Revisited

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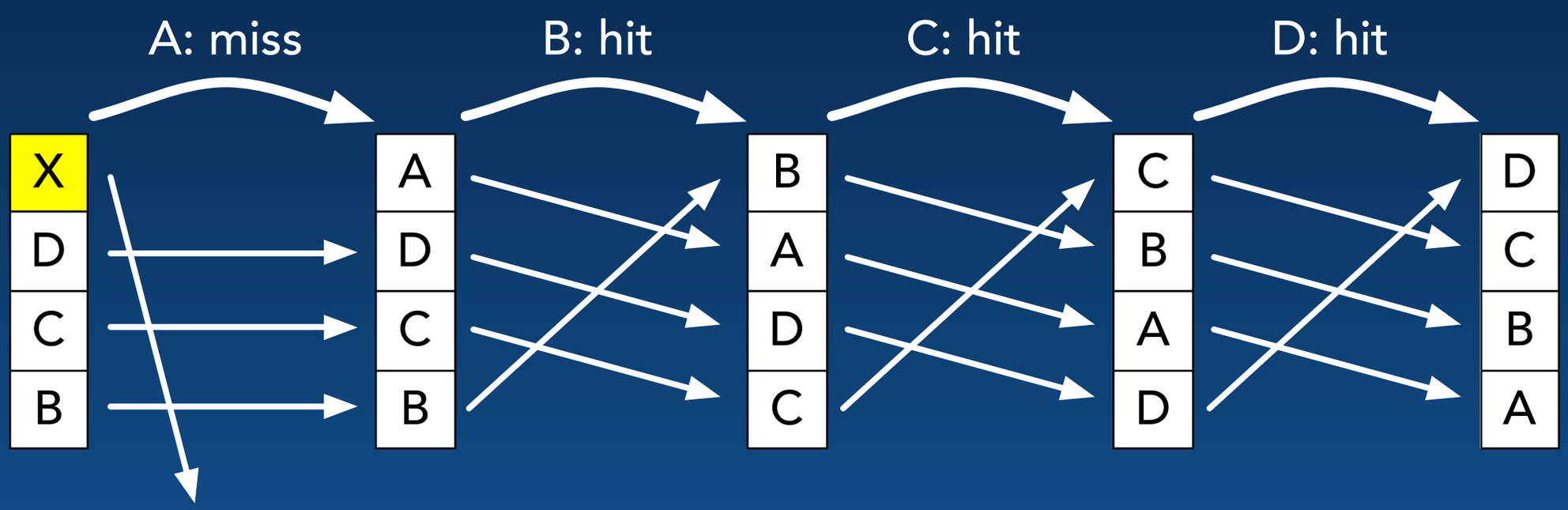

➡ No reordering misses

Selfish-LRU: Properties

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Property 1:

Selfish-LRU does not exhibit reordering misses.

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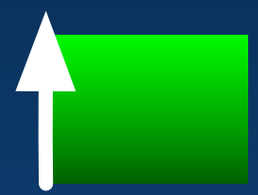
Property 2:

In non-preempted execution, Selfish-LRU = LRU.

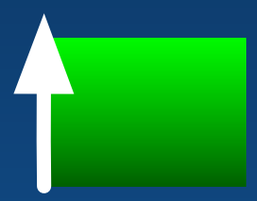
➡ No change in "regular" WCET analysis

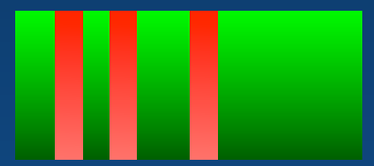
Selfish-LRU: CRPD Analysis

Preempting



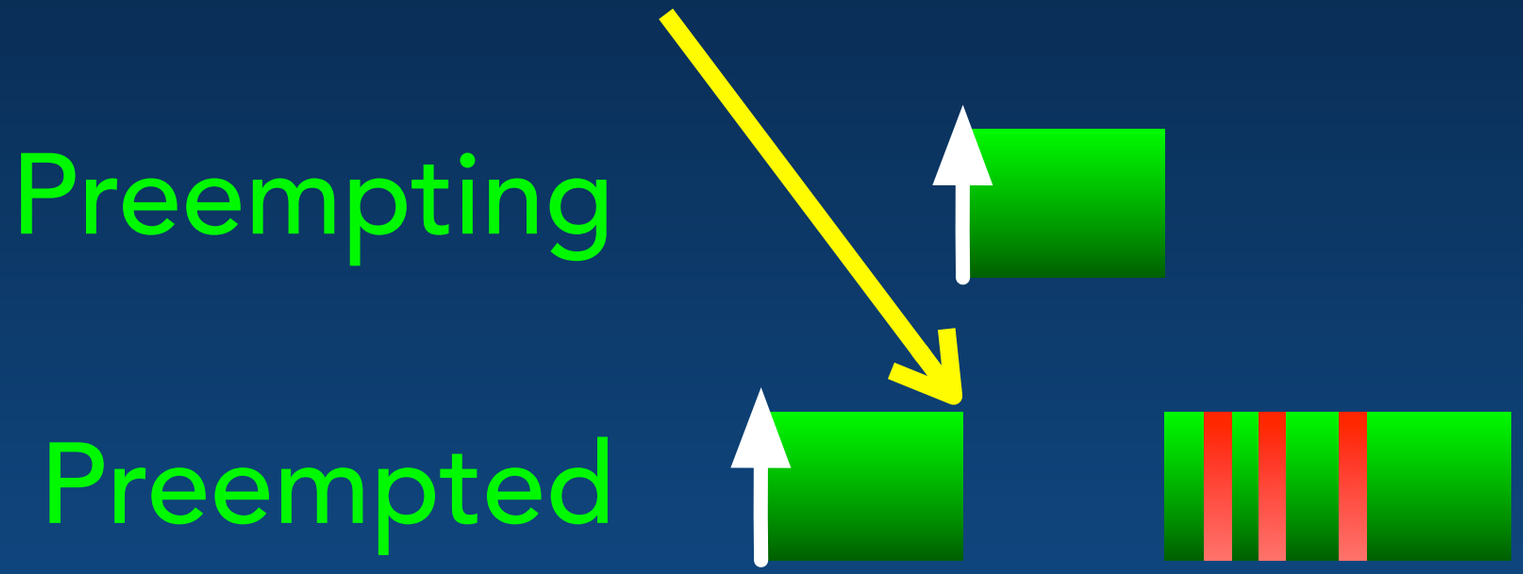
Preempted





Selfish-LRU: CRPD Analysis

1. Number of **useful cache blocks (UCBs)**?



Selfish-LRU: CRPD Analysis

1. Number of **useful cache blocks (UCBs)**?

2. Number of **evicting cache blocks (ECBs)**?

➡ Smaller Bound

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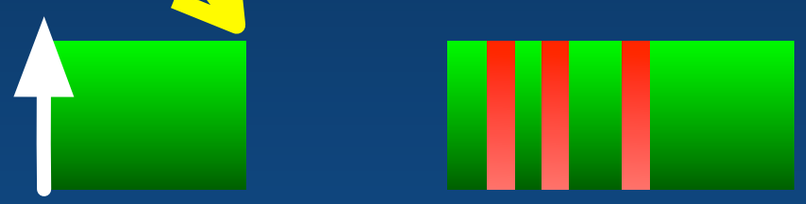

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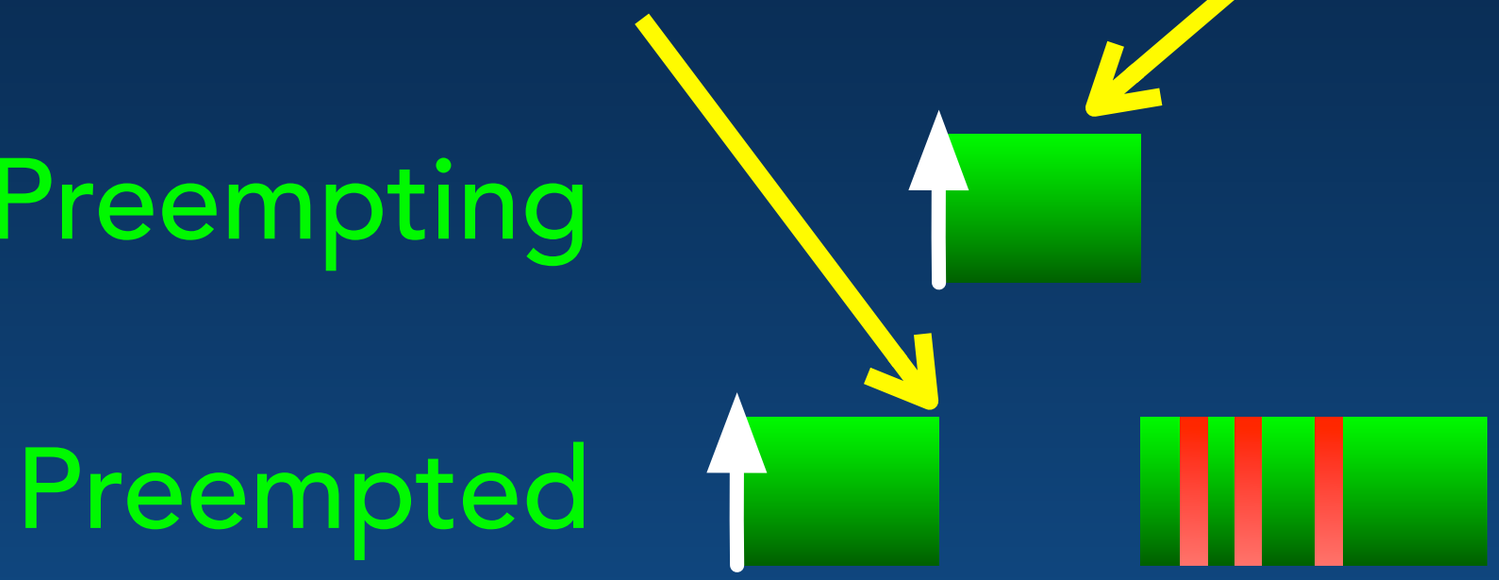

3. Combination of ECBs and UCBs based on **Resilience**

➡ Simplified and Smaller Bound

Selfish-LRU: Implementation

Required modifications:

- Manage **task ids (TID)** in operating system
- Make TID available to cache in **TID register**
- **Augment cache lines** with TID of "owner" task
  - Conservative estimate: < 3% space overhead
- Modified replacement logic

Similar to virtually-addressed caches

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Compare Selfish-LRU with LRU in terms of **performance** and **predictability**

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Secondary goal: (see paper for details)
Compare CRPD approach with cache partitioning

Experimental Evaluation: Benchmarks and Cache Configuration

Benchmarks:

- Four of the largest Mälardalen benchmarks
- Four models from the SCADE distribution
- Two SCADE models from an embedded systems course

Cache configuration:

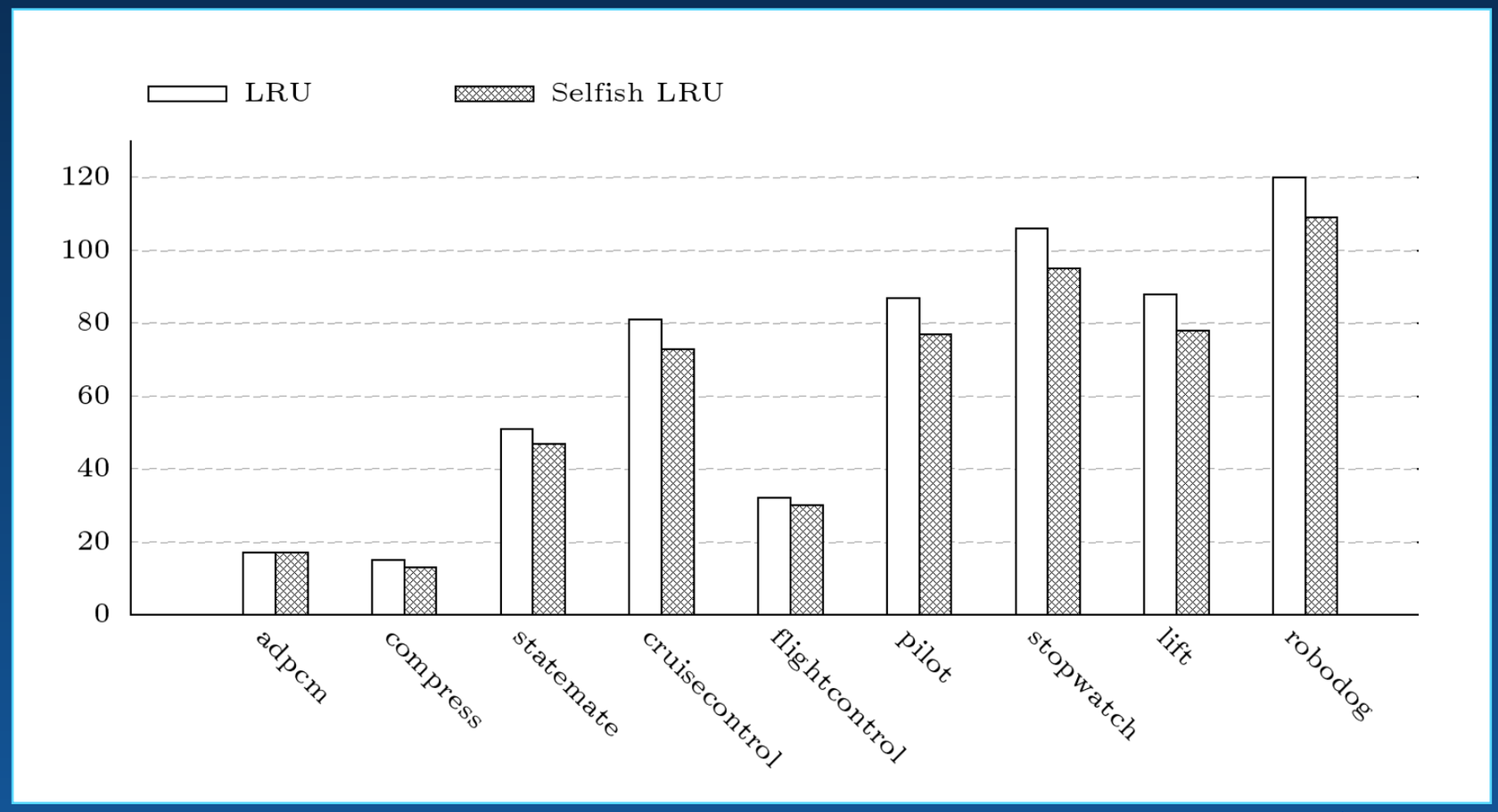
Capacity:	2 KB, 4 KB, 8 KB
Associativity:	4, 8
Number of sets:	32, 64, 128

Experimental Evaluation: Simulation Results, "Large" Preempting Task

Cache configuration:

Capacity: 2 KiB, Associativity 4, Number of sets: 32

Measured number of additional misses



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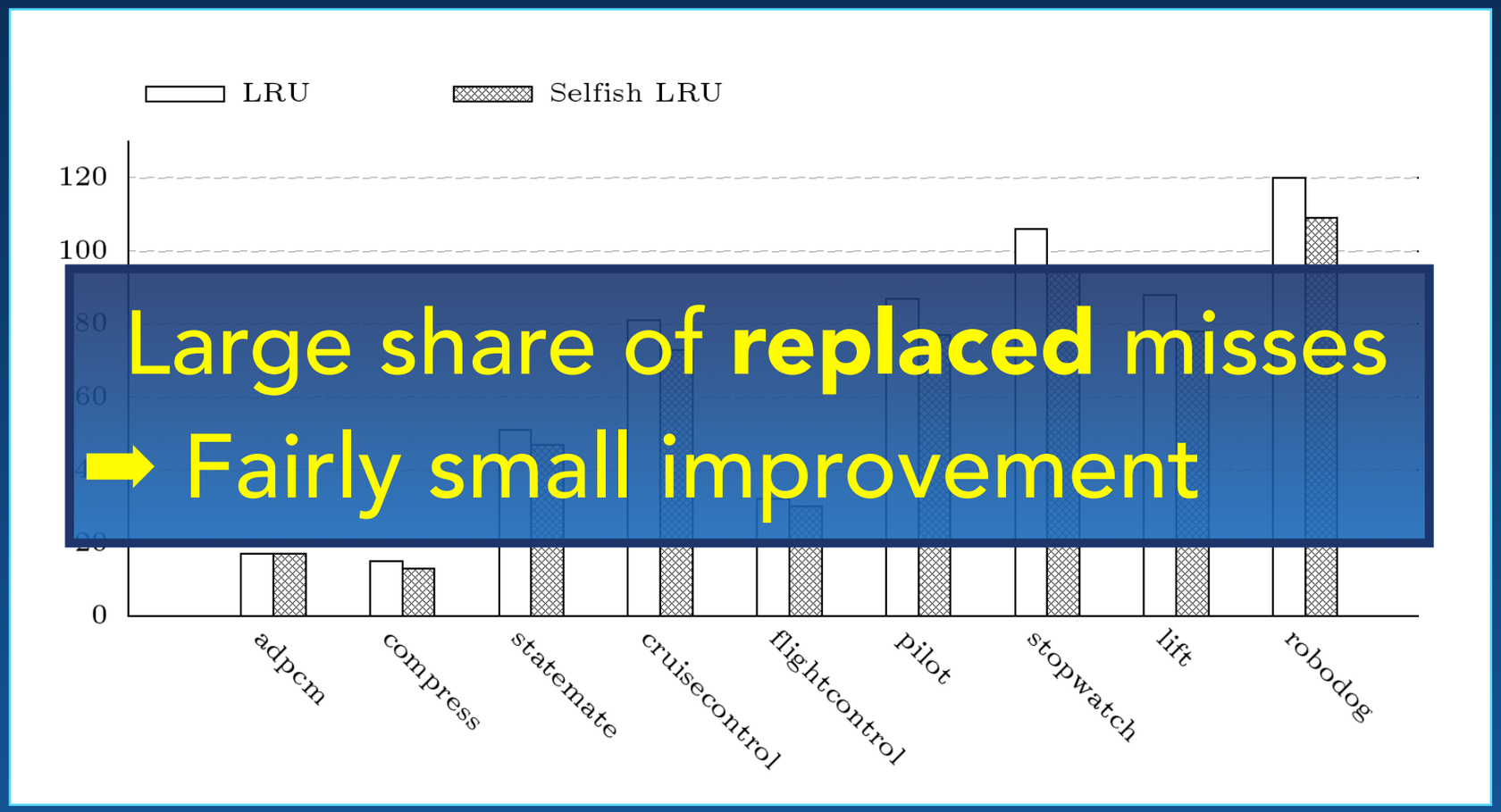

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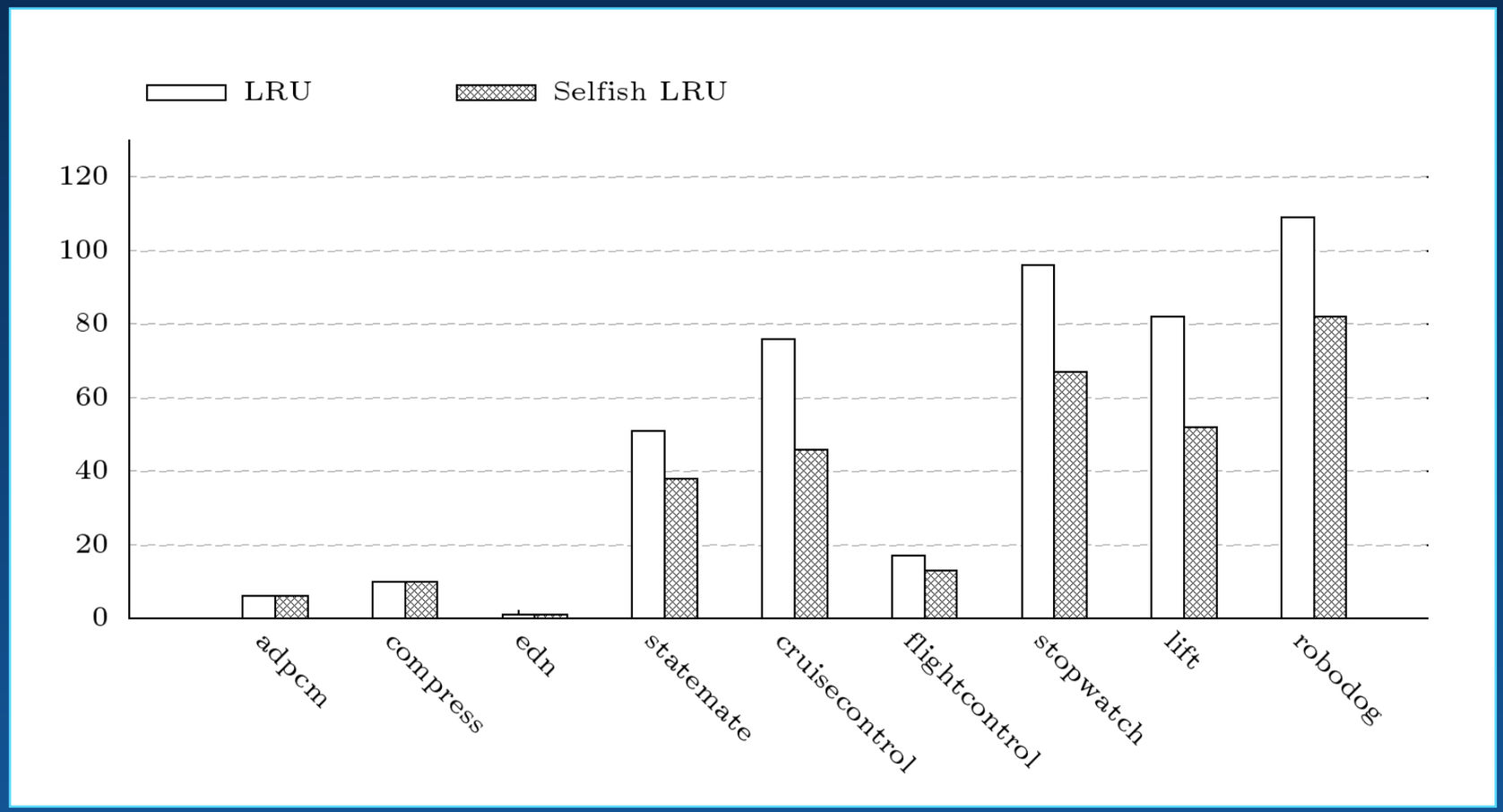

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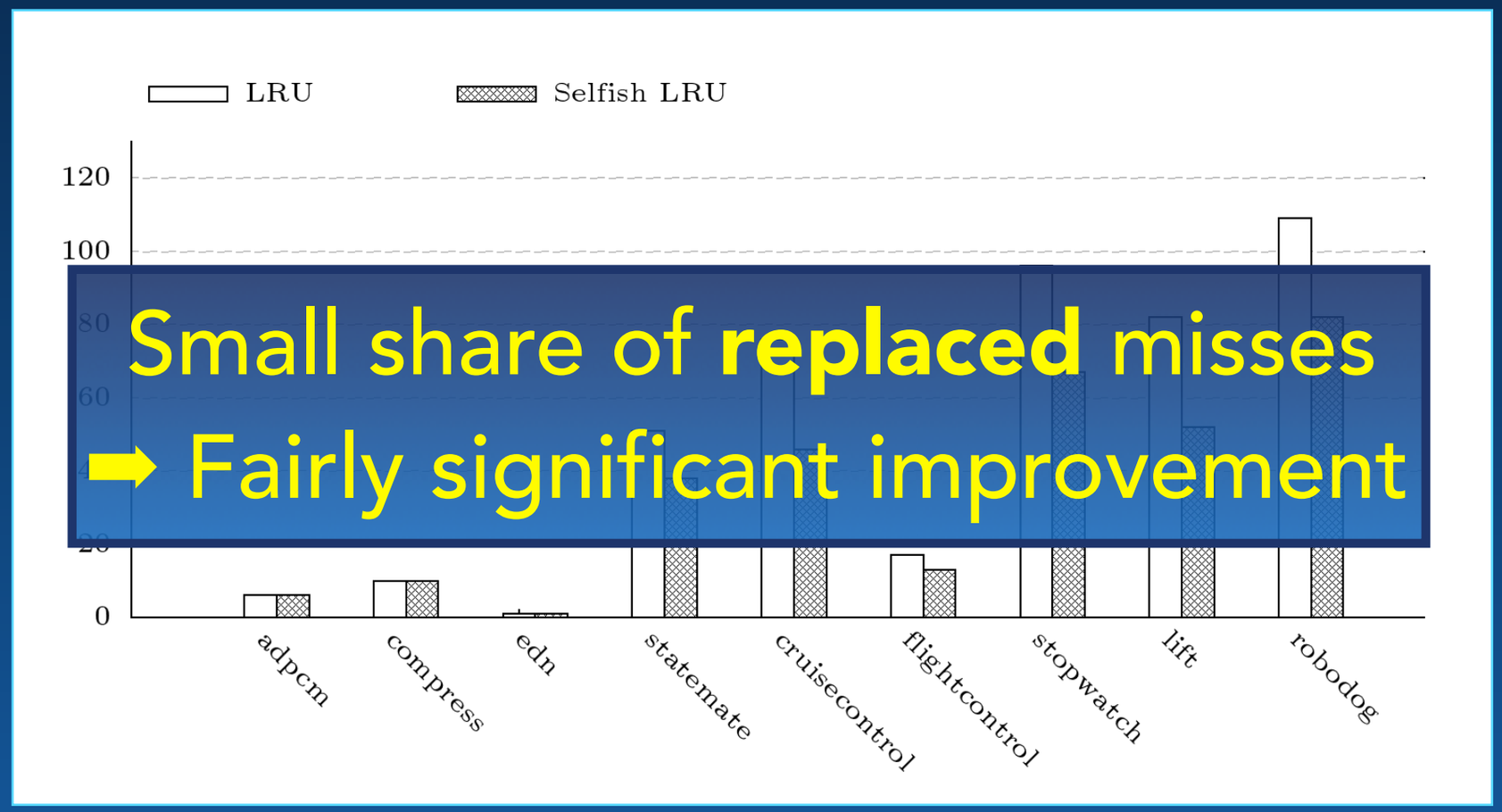

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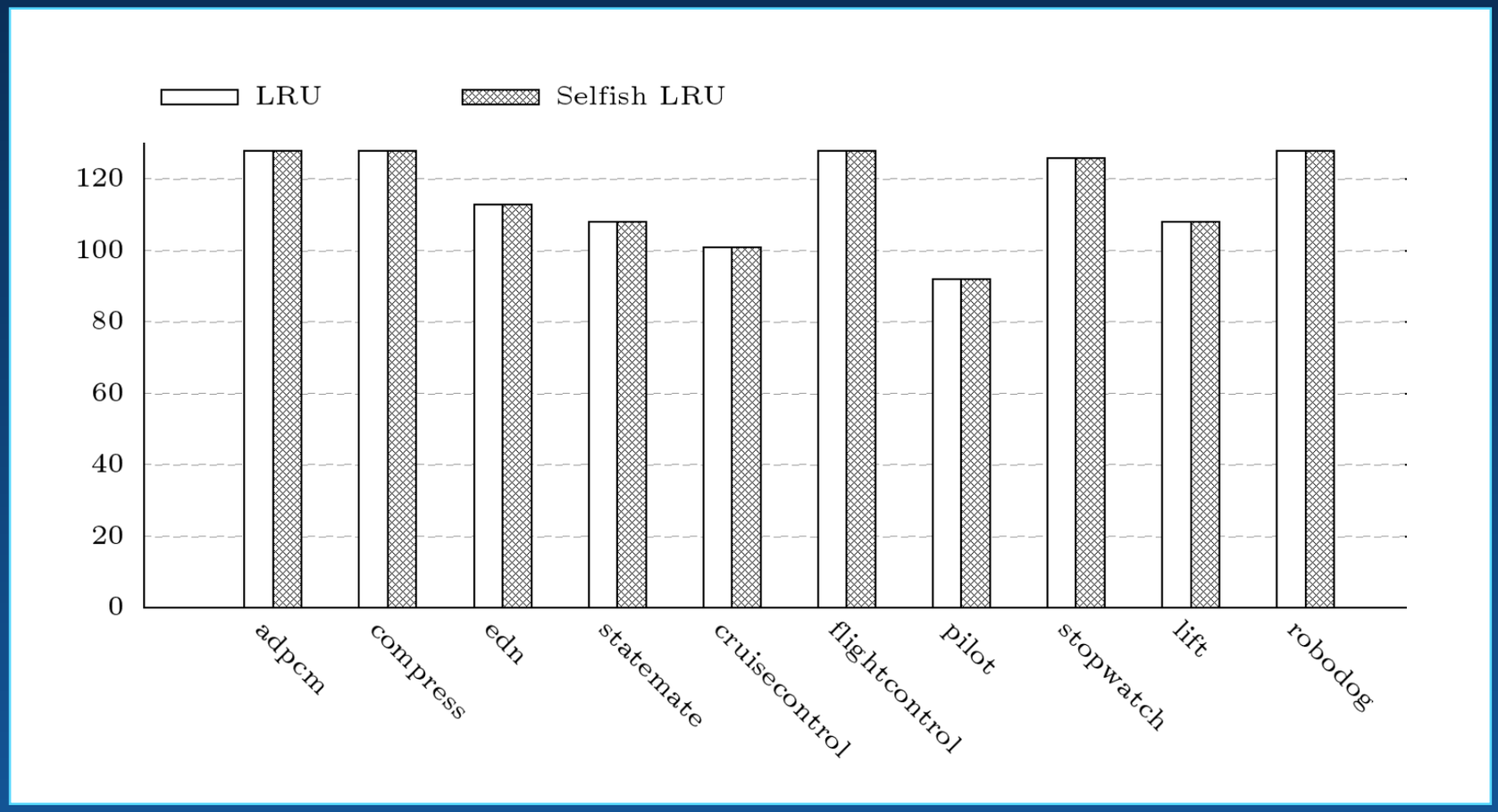

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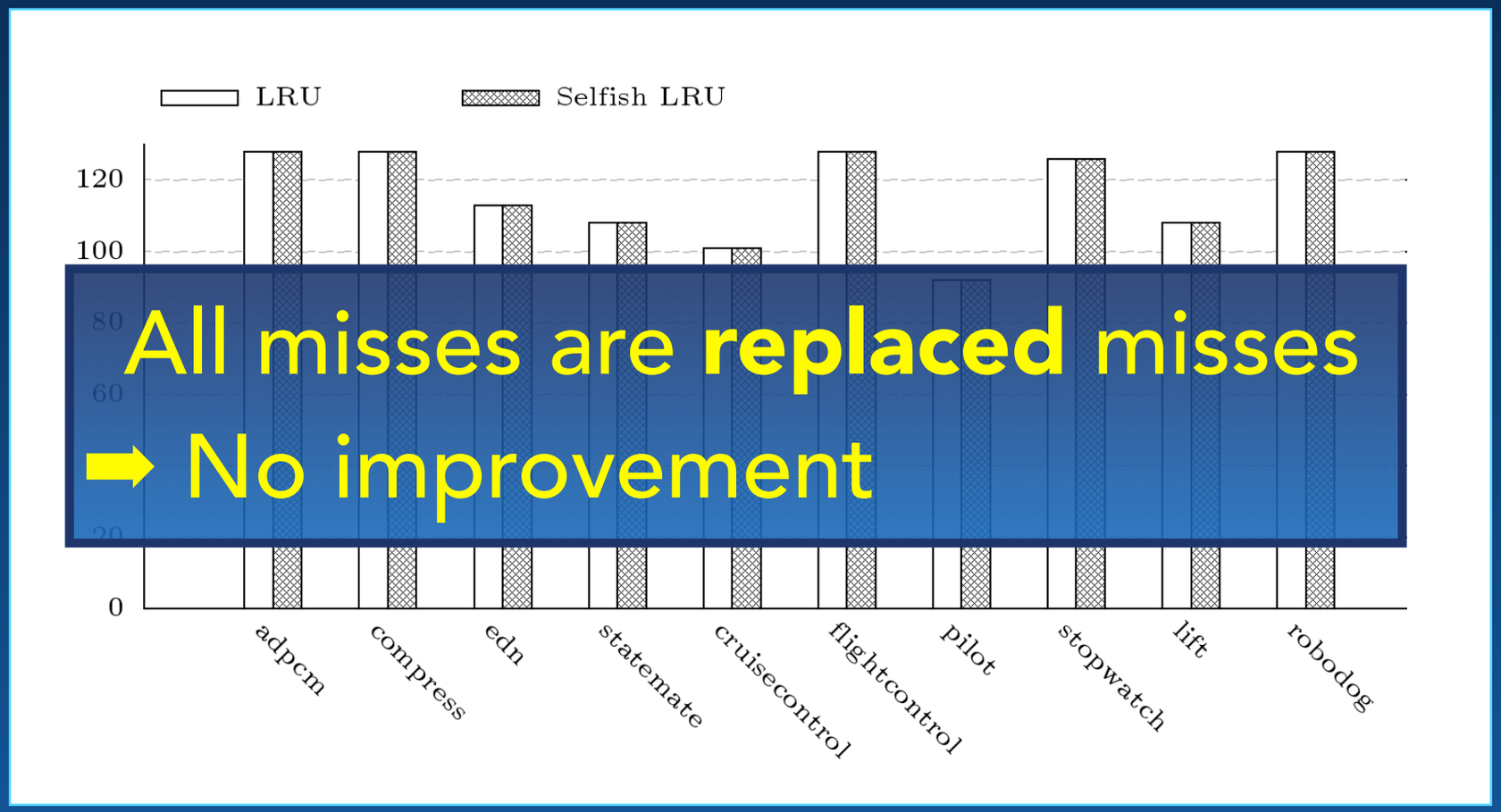

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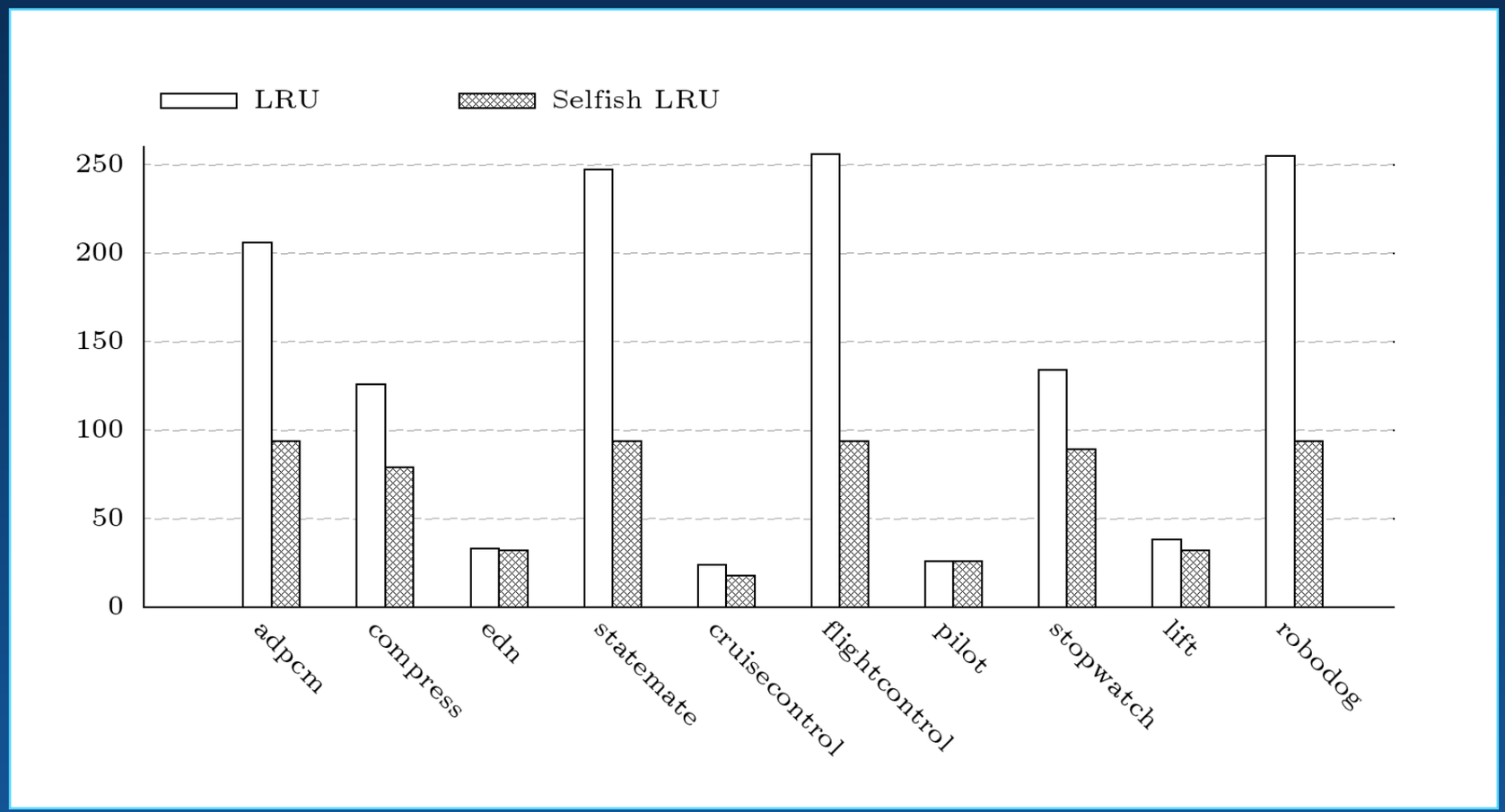
Cache configuration:

Capacity: 4 KiB, Associativity 8, Number of sets: 32

Bound on number of additional misses



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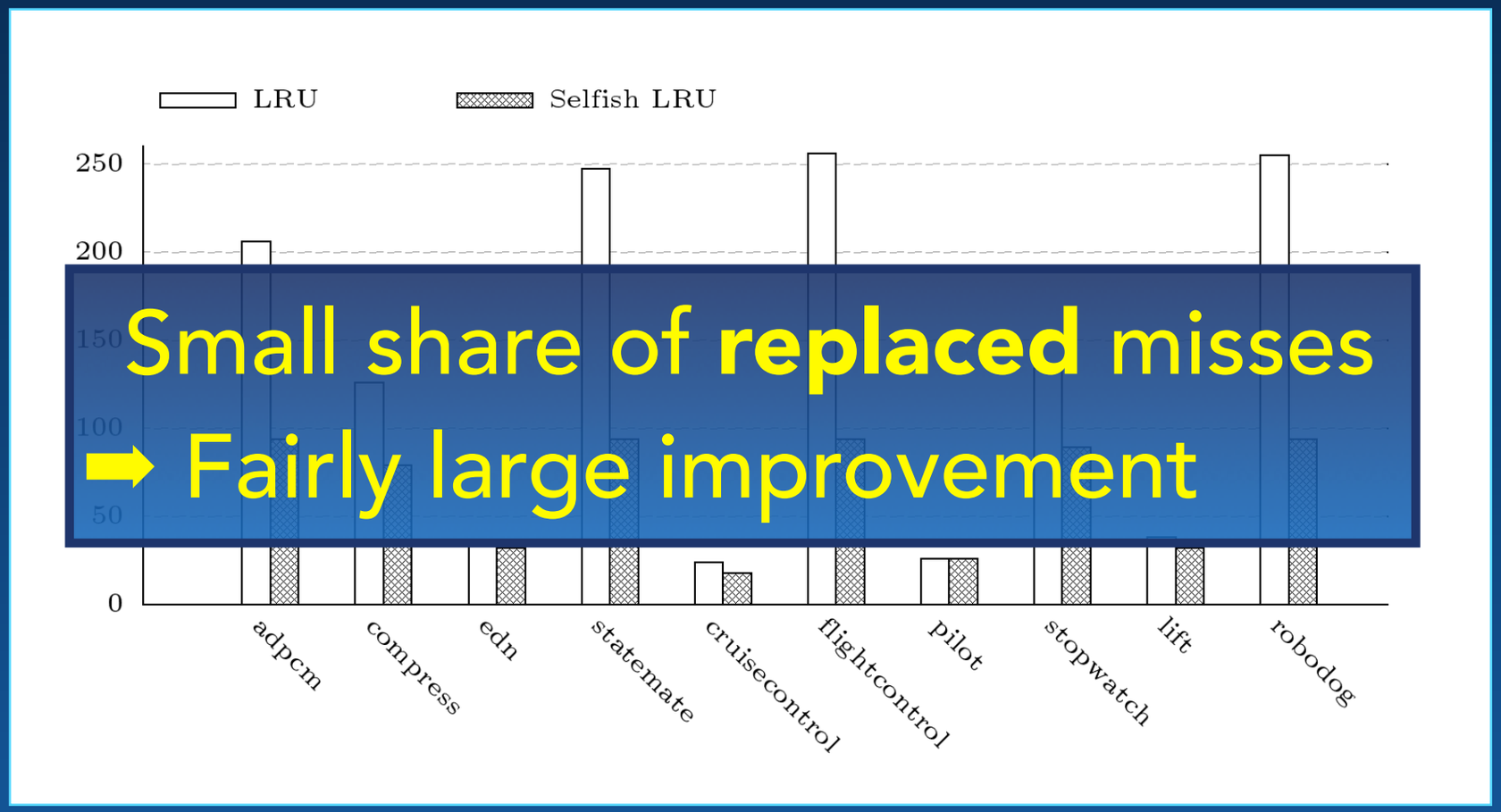

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Summary and Future Work

Selfish-LRU eliminates reordered misses:

- ➡ Increases performance by *reducing* the CRPD
- ➡ *Simplifies* static analysis of the CRPD
- ➡ Large improvements for small preempting tasks like interrupt handlers

Summary and Future Work

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Apply same idea in **shared caches** in multi-cores?